MONOLITHIC MICROFABRICATED ION TRAP FOR QUANTUM INFORMATION PROCESSING

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MONOLITHIC MICROFABRICATED ION TRAP FOR QUANTUM INFORMATION PROCESSING

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TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

To my loving and supportive wife

Samina,

and sweet children

Sachal and Saarang.

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SUMMARY

The objective of this research is to design, fabricate, and demonstrate a microfabricated monolithic ion trap for applications in quantum computation and quantum simulation. Most current microfabricated ion trap designs are based on planar-segmented surface electrodes. Although promising scalability to trap arrays containing ten to one hundred ions, these planar designs suffer from the challenges of shallow trap depths, radial asymmetry of the confining potential, and electrode charging resulting from laser interactions with dielectric surfaces. In this research, the design, fabrication, and testing of a monolithic and symmetric two-level ion trap is presented. This ion trap overcomes the challenges of surface-electrode ion traps. Numerical electrostatic simulations show that this symmetric trap produces a deep (1 eV for $^{171}Yb^{+}$ ion), radially symmetric RF confinement potential. The trap has an angled through-chip slot that allows back-side ion loading and generous through laser access, while avoiding surface-light scattering and dielectric charging that can corrupt the design control electrode compensating potentials. The geometry of the trap and its dimensions are optimized for trapping long and linear ion chains with equal spacing for use with quantum simulation problems and quantum computation architectures.

CHAPTER 1

INTRODUCTION

Quantum information processing has been shown theoretically to significantly enhance computing speed for specific engineering and scientific problems. Quantum information processing using trapped ions is a favored scheme among a number of experimental implementations of quantum processing because of the following reasons:

- it offers state initialization with high fidelity,
- internal and external qubit manipulations are well-controlled,
- coherence times are much longer that the typical quantum operations,
- qubit-specific read-outs can be done efficiently,
- qubits can be transported and structured in linear chains for a variety of quantum computation and simulation experiments.

Many quantum simulation experiments require stable linear ion chains. To trap long ion chains of 20 or more ions, the ion traps have to be small (DC electrodes widths in 100 μm range) with the flexibility of designing specific geometric configurations. Microfabricated surface-electrode traps offer such flexibility and scalability but lack in key trapping characteristics such as trap depth and the radial confinement symmetry. This thesis demonstrates a novel, hybrid design of a micro-scale ion trap. The ion trap design is the hybrid of a two-level structure and the planar electrode geometry. The two-level structure gives it a superior trapping depth and radial confinement symmetry as compared to the micro-scale surface-electrode traps, while the planar electrode geometry retains the flexible design geometry that surface-electrode traps have to offer. The ion trap is monolithic and is fabricated using standard Si-based CMOS processes. Both of these properties make the fabrication more robust, uniform, and reproducible.

In this thesis work, I present the concept of the symmetric trap by presenting both a single-ion and linear ion-chain simulation studies. The geometry is designed specifically for the linear chain quantum simulation experiments that use Raman beams for transversal-mode coupling between ions in a chain. I describe the fabrication of this trap using Si-based CMOS processes. A limited set of semiconductor tools was used to make it a more achievable device in standard fabrication facilities. Furthermore, I demonstrate the symmetric trap's trapping characteristics by experimentally trapping ions and measuring the stray fields and radial modes that confirm the simulation studies.

1.1 Outline of the thesis

This thesis describes the design, fabrication, and experimental demonstration of the symmetric trap. The thesis is divided into seven chapters organized as follows.

In Chapter 2, I present an introduction to the quantum information processing (QIP) with trapped ions. The chapter starts with a background and a quick history of QIP and reviews the fundamentals of quantum computation and quantum simulation. Describing the physical realization requirements for a quantum computer, I provide an overview of some of the most common physical schemes being explored for quantum computation. The rest of the Chapter 2 is dedicated to the introduction to quantum computation and simulation with the trapped ions. I conclude the chapter with presenting a summary of the recent quantum simulation experiments that set the stage for the motivation behind development of the symmetric trap.

In Chapter 3, an introduction to ion traps that are used for QIP is presented. I also describe the confinement principles of the Paul trap. The symmetric trap described in this thesis is a modified and miniaturized version of the Paul trap. Reviewing the literature, I present three main classes of the linear Paul traps that are microfabricated by several research groups. After discussing the two-level, three-level, and surface-electrode traps, I

present the design considerations for the microfabricated traps. These design considerations set the figures of merits for the trap design that is presented in this thesis.

In Chapter 4, my work on the stability analysis of the asymmetric surface-electrode traps is discussed. In asymmetric surface-electrode traps the ion motions in two radial axes are coupled that break down the conventional ion stability analysis. Using a perturbative approximation method I derive formulas which describe the boundaries of the stability diagrams for the ion motion in radial directions.

In Chapter 5, I discuss the motivation and overview of the symmetric trap design. Describing the geometry and the trap dimensions, I discuss the merits of each geometrical aspect. I present a single $^{171}Yb^{+}$ and $^{40}Ca^{+}$ simulation results. I conclude the chapter with a presentation of our chain optimization algorithm with 20-ion and 50-ion linear chain simulation results.

Chapter 6 details the fabrication steps, recipes, and processes. Starting with the choice of materials, I describe the process of each level. In describing each deposition and etching layer, I present the mask layouts, 3D drawings of the structure build-up, and the corresponding process recipes.

In Chapter 7, the experimental setup to test the symmetric trap is presented. I present the designs of several ultra high vacuum (UHV) components that are used to build the UHV chamber to test the symmetric trap. I also describe the details of the laser layout and other important components of the experimental setup such as, collection optics, RF resonator, and DC voltage supply.

In Chapter 8, I present four experiments and corresponding results. Along with the trapped ion's images, I present measured stray fields and radial modes of the trapped ion in the symmetric trap. I conclude with recent modifications in the experimental setup for ongoing experiments using the symmetric trap.

Lastly, Chapter 9 concludes my thesis by summarizing the important learning from this research work.

CHAPTER 2

QUANTUM INFORMATION PROCESSING WITH TRAPPED IONS

2.1 Introduction

The seed of the quantum information processing (QIP) can be traced back to the attempt of P. Benioff [1] to describe a classical computation process with a quantum mechanical Hamiltonian and represent that description using a quantum Turing machine. A few years later, Richard Feynman in his 1986 lecture [2] described a basic model of a quantum mechanical computer and analyzed the limits of classical computers in dealing with the quantum mechanical problems. During the same year, Deutsch [3] put forth the idea of universal quantum computer and described [4] a circuit model of a quantum computer that could surpass the computational abilities of any Turing machine. Later in 1993, Yao [5] connected the dots by showing that a quantum circuit model is equivalent to a quantum Turing machine. However, it was not until Peter Shor proposed a factoring quantum algorithm [6] in 1994 that the rapid development of QIP began. This algorithm used quantum computing principles to solve the problems of discrete logarithms and factorization in a number of steps which is polynomial in the input size as opposed to the classical algorithm which grows exponentially with the input size. The Shor's algorithm running time is $O(n^3)$ as compared to a best-known classical algorithm with running time which grows $\exp(O(n^{1/3}(\log n)^{2/3}))$. With the advent of Shor's algorithm, more algorithms were developed that exploited the powers of quantum mechanics. Some followed the ideas from Shor's algorithm period-finding, others like Grover's search algorithm used quantum superposition giving a quadratic speed-up as compared to best classical search algorithm $O(n) \rightarrow O(n^{1/2})$ [7].

With the conceptual proposals of Feynman, Deutsch, and Benioff, and algorithmic proposals of Shor and Grover, other theoreticians and experimentalists started looking into

the possibilities of experimentally implementing controllable quantum systems. Since then quantum information science has emerged as a research area that deals with storing, transmitting, and processing information using quantum bits. This emergence is mainly motivated by the need for understanding the physics of quantum systems and their computing potential. The possibility of technological advances such as room temperature superconductivity has stimulated interest in quantum simulation of condensed matter systems. Innovations and progress in the fields of lasers, vacuums, and nano-systems have enabled scientists to conduct complex experiments that would not have been possible without the renewed interest in QIP. A number of experimental groups worldwide are using a wide variety of technologies to implement QIP, e.g. trapped ions, neutral atoms, Josephson junctions, and photonic systems, to implement useful quantum information processors.

The unique resources for quantum computation come from the superposition and entanglement properties of quantum mechanics. Quantum information is described using the notation of a qubit (quantum bit). A qubit is considered to be in the state $|0\rangle$, $|1\rangle$, or superposition $\alpha|0\rangle + \beta|1\rangle$. The qubit's state evolves during a quantum process by being acted on by quantum mechanical operators. These operators act in general on the superposition state $\alpha|0\rangle + \beta|1\rangle$. For n qubits systems the number of possible terms describing the quantum state grows as 2^n. To get an idea of the scale of this increase in the information possible in a n-qubit system, we can see that for 500 qubits, $n = 500$, the number of terms necessary for a complete description of the quantum system will be $2^{500} \approx 10^{150}$, a number which is much bigger than the number of particles in this universe, or the age of this universe in femtoseconds. In fact, it is much bigger than the product of these two quantities.

Entanglement between qubits in a multi-qubit processor is a key to the speed-up possible with quantum processors and simulators. The secret of this entanglement lies in the linearity of the quantum mechanical operators which give rise to the tensor product required to describe the combination of two Hilbert spaces. When measurements are performed on

two qubits, each having its own associated Hilbert space, the tensor product results in correlations between the two qubits. The density operator ρ provides a useful way to describe a quantum state $|\psi_i\rangle$ that is not completely known,

$$\rho = \sum_i p_i |\psi_i\rangle\langle\psi_i| \, . \tag{1}$$

If a state is completely known so that $\rho = |\psi\rangle\langle\psi|$, it is referred to as a *pure state*. Otherwise the state is considered to be in a *mixed state*, a statistical ensemble of pure states with probabilities p_i for the component states. For a pure state $tr(\rho^2) = 1$ and for a mixed state $tr(\rho^2) < 1$, where tr denotes the trace operation. If two quantum systems have pure states $|\lambda\rangle_1$ and $|\phi\rangle_2$ and if their composite state $|\psi\rangle$ is a state that cannot be written as product state, i.e. $|\psi\rangle \neq |\lambda\rangle_1|\phi\rangle_2$, then the state is entangled. A direct test of entanglement in a composite state is provided by taking a partial trace of the density operator (ρ) over one of the sub-systems that comprise the composite system. Suppose the composite density operator of system 1 and 2 is ρ as given in (1). Taking a partial trace over system 2 gives the reduced density operator of first system $\rho_1 \equiv tr_2(\rho)$. For an entangled state $tr(\rho_1^2) \neq 1$. For an entangled state of two systems with orthonormal sets $|\lambda_i\rangle$ and $|\phi_i\rangle$ for system 1 and 2, consider two operators $\hat{A}$ and $\hat{B}$ representing physical observables whose eigenstates are $|\lambda_i\rangle$ and $|\phi_i\rangle$ states such that

$$\hat{A} = \sum_i \lambda_i |\lambda_i\rangle\langle\lambda_i|$$
$$\hat{B} = \sum_i \phi_i |\phi_i\rangle\langle\phi_i| \, ,$$

where λ and ϕ are eigenvalues of corresponding operators, then the measurement of $\hat{A}$ uniquely determines the outcome of $\hat{B}$. If the two states are completely entangled the two observables are perfectly correlated.

The role of the entanglement and its usefulness in quantum computation is being explored by many computer scientists and mathematicians. The role of entanglement has been under debate since the amazing potential of quantum computing was first proposed.

Josza and Linden proved a very important theorem, that multi-qubit entanglement is a necessary but not sufficient requirement for a pure-state quantum computing algorithm to offer an exponential speed-up over a classical computer [8]. They suggested that mixed-state algorithms might not necessarily require multi-qubit entanglement or can provide speed-up even with a small amount of entanglement. This reasoning was elaborated further by Kendon and Munro [9]. They showed that mixed-state quantum computing can require exponential resources to be simulated on a classical computer even in the absence of any entanglement among qubits. Along the lines of [8], they also proved that, for Shor's algorithm to offer exponential speed-up, there has to be an increase in entanglement as the algorithm evolves. They found this resource to involve the choice of basis for the quantum Fourier transform. Similarly, Grover's algorithm relies on pure-state entanglement as proved by Biham et al. [10]. All of this work, however, does not imply that the systems are classical in the absence of entanglement as discussed in [11]. There are proposals for a measure of quantum correlation by another phenomenon called quantum "discord." These proposals utilize discord in mixed-state quantum computing experiments [12, 13].

The quantum computers are envisioned to be able to exceed the capabilities of classical computers in the following two classes of problems [14]:

- To solve problems having properties that can be exploited using algorithms similar to Shor's and Grover's algorithms. Shor's algorithm relies on finding periodicity and Grover's algorithm relies on searching large spaces.

- Simulating and exploring quantum systems efficiently and more precisely.

Given these two classes of problems, recent efforts have focused on developing quantum computers to solve the problems similar to factorization using quantum algorithms and to simulate quantum phenomena using a quantum simulator.

2.1.1 Quantum computation

Learning from the foundation of circuit-based computation used for classical digital computers, quantum computers are being conceptualized to rely on the concepts of universal gates and circuits. In the field of computer science, much effort is focused on analyzing a problem and reducing it to a category of problems whose solution is either known, or can be found using some other algorithm. Using a similar approach, the development of quantum computers relies not only on the development of the design elements using algorithms that can be implemented but also on algorithms that can either be represented by a known algorithm (reduction of problems to utilize the period-finding and large-space search) or directly utilize the design elements.

Quantum gates, analogous to the digital gates of classical computers, act upon Boolean elements, the quantum bits (qubits). In QIP, the information between preparation and the final measurement remains in a quantum state that evolves under the influence of a system Hamiltonian. This Hamiltonian can be represented by one or multiple unitary operations (gates) which are capable of evolving the system in same manner as the Hamiltonian of a quantum system that is being simulated. The goal of QIP is to control and engineer this evolving system under the influence of unitary transformations in order to achieve a useful computation [15]. A generic graphic representation of a unitary gate on a single-qubit is shown in Figure 1.

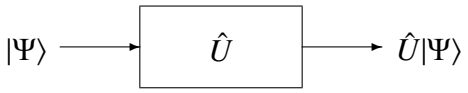

Figure 1: Generic representation of a unitary transformation as a quantum gate.

Quantum gates can operate on a single qubit or multiple qubits. Similar to the case for a classical computer for which the universal digital gates are NAND, NOR, and NOT, there are universal quantum gate sets containing both single-qubit quantum gates and multiple-qubit quantum gates. They are called universal in the sense that all other complicated gates

and operations can be implemented using these universal gates. There is one major distinction between multi-qubit quantum gates and classical gate sets. A two-qubit quantum gate does not transform two-qubits into one as it is in the classical case. Several single-qubit gates and a two-qubit quantum gate are shown, which are chosen on the basis of their usefulness in quantum algorithms are shown in Figure 2. These gates have corresponding unitary transformations and circuit diagrams. The gates shown in Figure 2 are not necessarily independent. Some of them can be a part of universal set of quantum gates. For example, the Hadamard and $\pi/8$ gates are single-qubit gates, the controlled NOT (CNOT) gate is a two-qubit quantum gate and together they form a universal quantum gate set. Careful examination of the CNOT unitary transformation of the CNOT gate reveals its quantum nature. The CNOT gate can entangle a pair of qubits. A ground state qubit $|0\rangle$ can be transformed by a Hadamard gate resulting in $\frac{1}{\sqrt{2}}(|0\rangle + |1\rangle)$. And then used as a control qubit for a CNOT transformation. If the target qubit for this CNOT transformation is a ground state $|0\rangle$ then the resulting state is an entangled state.

$$\hat{U}_{CNOT}\Big((\frac{1}{\sqrt{2}}(|0\rangle + |1\rangle)) \otimes |0\rangle\Big) = \frac{1}{\sqrt{2}}(|00\rangle + |11\rangle)\,, \tag{2}$$

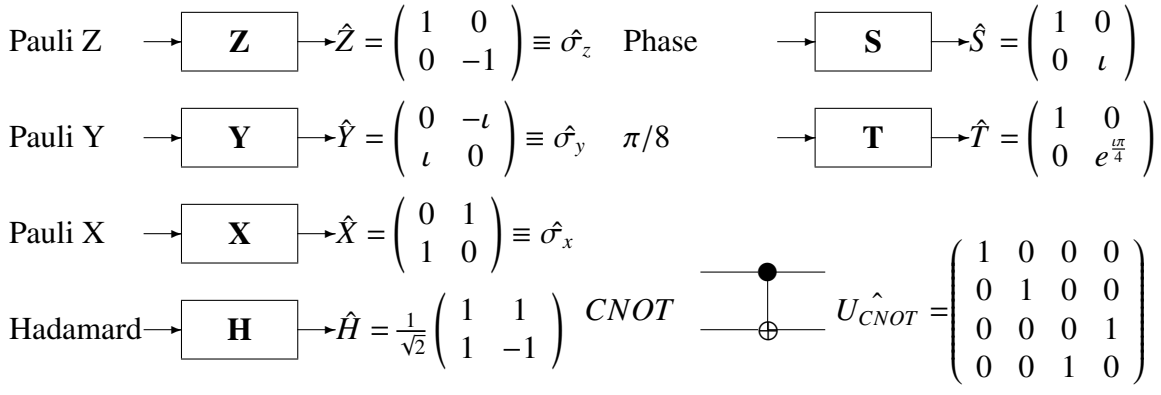

Figure 2: Most useful single-qubit and two-qubit quantum gates with corresponding circuit and matrix representations.

Quantum computation focuses on the mapping of a computational problem into an algorithm that can be broken down into a sequence of quantum gates which are physically

realizable with the least errors and fastest rates. Depending upon the physical system of the quantum processor, quantum gates are chosen and implemented to act as a specific component of the algorithm. The combination of operations can schematically be drawn in a circuit diagram - called a quantum circuit. In reality when quantum operations are performed they are prone to several kinds of errors due to decoherences caused by the interaction of the computation component with the environment and imperfect control parameters in the experiment. Based on extending Shannon's information theory for classical systems to quantum systems, Shor showed that the effects of the errors in a quantum information channel can be minimized by adding redundancy into the system [15]. This redundancy is typically included in quantum error-correction codes. A variety of quantum error-correction coding schemes have been proposed. A few of them have been demonstrated experimentally [16, 17]. For quantum computation to work, quantum error-correction schemes have to be robust and experimentally feasible to be incorporated into the computations while solving a problem. Building a universal quantum computer using quantum gates for the application of an arbitrary unitary transformation requires a significant amount of redundancy and built-in quantum error-correction.

2.1.2 Quantum simulation

Quantum simulation refers to mimicking one quantum system by another quantum system. Since Feynman's initial concepts of quantum simulations in 1985 [2], there has been rapidly growing interest in trying to simulate locally interacting closed and open quantum systems using another controllable quantum system [18]. Quantum simulation can be accomplished using several methods. One method is to apply the quantum operations which mimic a sub-system Hamiltonian in sequence, assuming each operation avoids decoherence. These operations can be engineered to achieve the desired evolution of the over-all system. The basis of another quantum simulation technique utilizes local interactions between components of a quantum system. This enables the system Hamiltonian to

be expressed as the sum of local Hamiltonians $H = \sum_{i=1}^{l} H_i$. In this case the *Trotter formula* and *BCH lemma* [19] can be applied and the simulation can progress by time-slicing the evolution so that $e^{\iota Ht} \approx \left(e^{\frac{\iota H_1 t}{n}} e^{\frac{\iota H_2 t}{n}} \ldots e^{\frac{\iota H_l t}{n}}\right)^n$, where the time slice is small enough and that the total Hamiltonian is expandable as the set of products. In this case the accuracy of an efficient simulation experiment can be calculated and found to be within achievable polynomial limits ($l = l(N)$) [18]. Since the system under consideration has limited local interactions (neighbor or nearest neighbor) we only deal with N variables. The same simulation on a classical computer involves exponentiation of 2^N X 2^N matrix, even if we use relaxation and estimation techniques of the Monte Carlo class.

When a Hamiltonian to be simulated is mapped into another controllable Hamiltonian that can be experimentally implemented, the system is referred to as an analog quantum simulator (AQS). Examples of problems that can be dealt by AQS include high-temperature-superconductivity, superfluidity, Mott insulators, ferromagnetism phase transitions, and spin-spin interactions [20]. Such problems can easily be reduced to the bosonic or fermionic interactions and can be modeled by Hubbard or Ising Hamiltonians. Implementing these systems, using a lattice of qubits such as ions or atoms, is in progress at present [21]. Implementing an AQS to solve problems that do not require high accuracy has less stringent error correction requirements than a universal quantum processor [22].

A digital quantum simulator (DQS) maps a Hamiltonian of a complex quantum system into quantum gates using circuit-based quantum computing. Since DQS is realized by using universal quantum gates, its universality gives it an advantage over AQS. However, the complexity of a DQS scales-up as the required accuracy increases [23].

2.2 Quantum processors requirements

The tremendous interest of the scientific community in the research area of quantum computing has brought many proposals for physical systems that can be used as a quantum

computer. In 2000, Devincenzo [24] put together the criteria required for a universal quantum computer as follows:

- **Well-defined qubit** - The system should have a well-defined and identifiable qubits. These qubits should be accessible so that they can be added to the processor as the computation progresses.

- **Initial preparation** - The quantum computer must be able to initialize the qubits to a pure state (typically the ground state). When dealing with a multi-qubit ground state, the system state can be represented by the tensor product of the individual qubit ground states $|0_1 0_2 \dots 0_N\rangle$.

- **Long coherence time** - There are several types of decoherences that can cause the qubit to couple to the environment. If these decoherences occur sooner than the operations are performed, the system will not be able to evolve as desired. Thus, the coherence time for the qubit has to much longer than the gate time.

- **Quantum gates** - The system should be able to implement a set of universal quantum gates. Since arbitrary unitary transformations can be represented by a set of universal quantum gates (by definition), the system should be able to implement any Hamiltonian if it has universal single- and two- qubit gates. Analog quantum simulators do not rely on universal quantum gates. They rely on quantum operations performed locally which can evolve the Hamiltonian of the quantum system.

- **Qubit-specific read-out** - There must be a reliable way to measure the state of the desired qubit(s). In essence Von Neumann measurements, which leave the system in the eigenstate corresponding to the measurement outcome, can be done to perform read-out.

2.3 Physical systems for quantum computation

The physical systems that are being explored for quantum computers span much of the modern physics field: quantum dots, superconducting Josephson junction, ions, neutral atoms, Rydberg states of atoms, photons, cavity quantum electro dynamics (cQED), nuclear magnetic resonance (NMR), single-electron-based qubit systems like nanotubes, fullerenes, graphene, and single-atom-based qubit systems like Si doped with Phosphorus atoms [25]. Before quantum computing with trapped ions is discussed in detail, it will be beneficial to summarize and provide an overview of the most promising technologies [15].

- In nuclear magnetic resonance (NMR), nuclear spin aligned parallel or anti-parallel to an applied magnetic field can act as a qubit. Unitary transformations are performed by resonant radio frequency pulses. Interactions between neighboring atomic nuclei can provide the source of entanglement.

- Neutral atoms can be trapped and cooled in optical or magnetic traps. The qubit can be coded into the electronic levels of each atom. Atoms can interact with other atoms to provide the coupling necessary for quantum computing. Rydberg states can also be used to encode qubits. Phenomena such as the Coulomb blockade can be used to couple the states between Rydberg atoms.

- In cQED, a single atom with qubit in its electronic level can be coupled to optical cavity modes. The atom can interact resonantly with an optical mode and emit a photon into the cavity. This coupling process can be used to induce coherent photon exchange between atoms.

- For quantum dots formed in semiconductor structures, the qubit is encoded into quantum dots' charges or its electron spins. Qubits can be coupled by applying electric fields on appropriate electrodes to bring electronic energy levels into resonance.

- Superconducting quantum processors rely on coupling of Cooper pairs in superconductors through Josephson junctions and Josephson tunneling between superconductor-insulator-superconductor (SIS) structures. Devices such as the superconducting quantum interference devices (SQUID) have quantized magnetic flux that can be used to encode qubits. These devices can be coupled through the flux to realize qubit interactions. Charge qubits are implemented using charge created by tunneling of the Cooper pairs through a Josephson junction. A phase qubit can be implemented by Josephson tunneling in a SIS.

2.4 Trapped ions

Trapped-ions are the most advanced and favored scheme for implementing quantum logic [19]. Ions can be easily trapped and cooled in well-controlled positions. Their internal states can be manipulated with lasers and can be measured with nearly 100% efficiency. The possibility of using trapped ions as a quantum computing scheme was first proposed by Cirac and Zoller in 1995 [26]. They proposed coupling the trapped ion's vibrational mode to the ion's internal degree of freedom. Soon after that Monroe et al. implemented this proposal by trapping a Be^+ ion and implementing the conditional phase-shift [27]. That experiment was followed by several successful experiments demonstrating two-qubit gates, four-particle entanglement [28], and decoherence-free subspace [29]. The groundwork for trapping an ion [30] in a Paul trap and the experiments demonstrating the excitation of an internal ion-level [31] and reading out the excited population [32] were conducted in the 1980s. Trapped ions fulfill the DeVincenzo requirements. Trapped-ions are also an attractive platform for quantum simulation experiments. Ions can be stored and cooled at specified positions to form various lattice shapes. Their internal states can be manipulated using lasers and microwaves to simulate local or long-range interactions using analog and digital quantum simulation schemes.

2.4.1 Qubit representation

In the trapped-ion platform, the qubit can be implemented using a two-level system such as electron's spin in a magnetic field, two electronic levels of an ion or hyperfine levels involving the ion's nuclear spins. Long coherence times are obtained by using the long-lived internal hyperfine levels. Long-range qubit interactions can be formed in linear ion chains through the low level vibrational modes (phonons) that arise through Coulomb interactions between the trapped ions. The qubits are initialized by optically pumping and cooling the trapped ions into their motional and hyperfine ground states. Fluorescent measurements of the hyperfine state or electronic level are performed for qubit read-out.

The qubit must have a long coherence time compared to the quantum operation time. For trapped-ions two different schemes are typically used to store the quantum information. The first scheme uses the two-level system provided by the electronic ground state and a metastable excited state. The coherence time for this scheme is slightly more than one second for Ca^+, Sr^+, and Ba^+ ions as compared to typical operation times of $0.1 \sim 500\mu s$ [33]. The second scheme is achieved using two hyperfine or Zeeman states within an electronic ground state. This scheme has a significantly larger coherence time than the first scheme and well above the requirements for any quantum information experiment. The first scheme is generally referred to as "optical qubit" and the second as an "RF qubit" or hyperfine qubit. These schemes are shown in a generic sketch in Figure 3. Optical and RF qubits coherence times are often limited by magnetic field fluctuations that vary the qubit level spacings. Several techniques have been engineered and employed to successfully isolate the qubits from magnetic field fluctuations to make coherence times long compared to manipulation time [33].

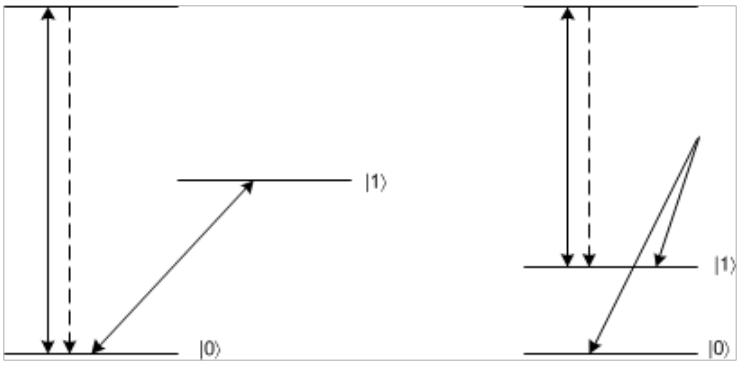

Figure 3: Generic level schemes of ions for optical (left) and RF (right) qubits.

The RF qubit can either be manipulated by microwave sources resonant with a hyperfine transition or a pair of Raman laser beams whose difference of frequencies is resonant with the hyperfine transition. The hyperfine level spacings are in the GHz range. For Raman excitation the two laser beams are tuned near a third level, typically an excited electron state. In the Raman process using anti parallel propagation of the two laser beams, an ion absorbs a photon from one laser field and emits a photon into a second laser field, transferring the two-photon recoil to the ion. The Raman process is somewhat forgiving in laser stability requirements since only the difference in the two laser frequencies needs to be stabilized at or near the hyperfine transition frequency. The Raman process adds A.C. Stark shift terms to the the total system Hamiltonian that must be accounted for in the quantum processing calculations.

The selection of the type of the ion is usually based on the availability of lasers required for the qubit transitions. The mass of the trapped ion plays an important role in determining the stability of the ion motion and corresponding operating conditions of the trap. The ions, Ca^+, Yb^+, Be^+, Mg^+, and Ba^+ have been popular choices. For $^{40}Ca^+$ an optical qubit utilizes the quadrupole allowed transition from ground S state to the meta-stable D state with a lifetime ~1 s while $^{171}Yb^+$ uses a qubit based on hyperfine state at 12.6 GHz. The intrinsic lifetime of this hyperfine state is $\sim 10^8$ s due to the low frequency and octupole nature of the transition. These two qubits in $^{40}Ca^+$ and $^{171}Yb^+$ are of primary interest for the research reported in this thesis.

2.4.2 Initialization and read-out

The qubits must be initialized in a well defined state before the implementation of a quantum algorithm. This initialization is typically achieved by optically pumping the trapped ion to a ground state of the two-level system representing the qubit. Optical pumping involves driving an ion into a selected excited stated until it decays completely into a desired state. Circularly polarized light is typically used to pump the ion into the desired ground state. Typically, the target state is nearly fully occupied in less than 1 μs with a probability larger than 0.99. The initialization fidelity is usually limited by the quality of the pumping laser polarization relative to the preferred axis of the qubit. In most cases, this axis is given by the direction of the magnetic field. To date the fidelities of 99.99 % have been demonstrated in [34].

At the end of a quantum algorithm the quantum register needs to be measured. This is typically achieved by exciting one of the qubit levels to a higher-lying auxiliary-short-lived level while the other qubit level remains untouched. The fluorescence from many cyclic state decays from auxiliary level is detected only if the qubit is projected to the qubit level which is coupled to the auxiliary transition. The photon detection is achieved through a small F-number ($\sim$ 1) lens system that collects the fluorescence light. The collected photons are counted using a photomultiplier tube. Several additional techniques have been incorporated to improve the detection efficiency. Recent experiments have achieved an average detection time of 145 μs with 99.99% accuracy [33].

2.4.3 Quantum gates

A combination of some single-qubit gates and a two-qubit gate make a universal set of quantum gates [19] e.g., single-qubit rotations and a two-qubit CNOT gate make a universal set of quantum gates. All quantum algorithms can be broken down into a sequence of operations consisting of the single-qubit gates and a specific two-qubit operation. In ion traps single-qubit gates such as the Pauli X and Pauli Y gates, shown in Figure 2, are implemented by driving Rabi oscillations between two qubit levels with resonant laser pulses.

The gates can be represented as rotations on the Bloch sphere where the axis of rotation is selected by changing the phase of the exciting laser field (single-photon transition) or the phase difference of the two Raman beams. A rotation transformation, $\mathfrak{R}$, acting on an internal-level qubit $\alpha|0\rangle + \beta|1\rangle$ has the form of a unitary gate

$$\begin{aligned} \mathfrak{R} &= \begin{pmatrix} \cos\theta & \iota \exp(-\iota\phi)\sin\theta \\ \iota \exp(\iota\phi)\sin\theta & \cos\theta \end{pmatrix} \\ &= \cos\theta \mathbf{I} + \iota \sin\theta(\hat{\sigma_x}\cos\phi + \hat{\sigma_y}\sin\phi) \end{aligned} \tag{3}$$

where $\theta = \frac{\Omega t}{2}$, Ω is the Rabi frequency (corresponding to the transition frequency,) and ϕ is the phase of the laser-pulse that sets the "axis of rotation" of the spin vector. A π-laser pulse ($\theta = \pi$) evolves the wave function through half a Rabi oscillation period and the state transforms from $|0\rangle$ to $|1\rangle$. A $\pi/2$-laser pulse takes a state $|0\rangle$ to $\frac{1}{\sqrt{2}}(|0\rangle + |1\rangle)$.

For a two-qubit gate Coulomb force between trapped ions is employed. This interaction causes the internal levels of two ions to be coupled through the trapped ion vibrational modes (external-level). Two internal-level qubits are represented in the standard basis as $|00\rangle$, $|01\rangle$, $|10\rangle$, and $|11\rangle$. The quantized vibrational mode can be in arbitrary state $|n\rangle$, where n is the harmonic oscillator level occupation number. A transition from a state e.g., $|00\rangle|n\rangle$ to $|01\rangle|n+1\rangle$ can be made by tuning a laser to the corresponding sideband frequency. These transitions provide a coupling between the internal and external modes. In the trapped-ion scheme this internal/external mode coupling provides a means to transfer the information between qubits and is referred to as a bus.

The Hamiltonian for a trapped ion can be written as

$$H = \hbar\Omega \{\hat{\sigma_+}e^{-\iota(\Delta t-\phi)} + \hat{\sigma_-}e^{\iota(\Delta t-\phi)} + \iota\eta(\hat{\sigma_+}e^{-\iota(\Delta t-\phi)} - \hat{\sigma_-}e^{\iota(\Delta t-\phi)})(\hat{a}e^{-\iota\omega_t t} + \hat{a^\dagger}e^{\iota\omega_t t})\}, \tag{4}$$

where Ω is the Rabi frequency, Δ is the laser detuning from the resonance, ω_t is the trap frequency, $\hat{\sigma_+}$, $\hat{\sigma_-}$ are raising and lowering operators for the internal qubit levels, and $\hat{a}$, $\hat{a}\dagger$ are creation and annihilation operators for the external motional mode. Here, the Lamb-Dicke approximation ($\eta\sqrt{\langle(\hat{a}+\hat{a}\dagger)^2\rangle}$) $\ll 1$ is used, which implies that the "creation" and

"annihilation" operators ($\hat{a}$ and $\hat{a}\dagger$) only cause single mode excitation or decay. In other words, the coupled ions will have either one phonon added to the system or taken away from the system. The ion energy spectrum exhibits resonances at $\Delta = 0$ and $\Delta = \pm\omega_t$. The resonance $\Delta = 0$ is the "carrier" resonance, and in this case only the terms with $\hat{\sigma_+}$ and $\hat{\sigma_-}$ will survive with the Rabi frequency being Ω. At the carrier resonance only the ion's internal-level (qubit) will be excited, $|0\rangle \rightarrow |1\rangle$. At the resonance $\Delta = +\omega_t$, the coupling term survives and the ion's vibrational mode will be excited from $|n\rangle$ to $|n+1\rangle$ (a phonon added to the system) with a Rabi frequency of $\Omega_{blue} = \sqrt{n+1}\eta\Omega$. In this case internal-level transition $|0\rangle|n\rangle \rightarrow |1\rangle|n+1\rangle$ is excited. This is a blue sideband resonance and can be used to "create" or excite the vibrational mode. The resonance $\Delta = -\omega_t$ is red sideband and is used to "annihilate" a vibration mode from $|n\rangle$ to $|n-1\rangle$ (a phonon taken away from the system) with Rabi frequency $\Omega_{red} = \sqrt{n}\eta\Omega$. In this case the internal-level transition $|0\rangle|n\rangle \rightarrow |1\rangle|n-1\rangle$ is excited. The sideband transition spectrum is schematically shown in simplified energy-level diagram in Figure 4.

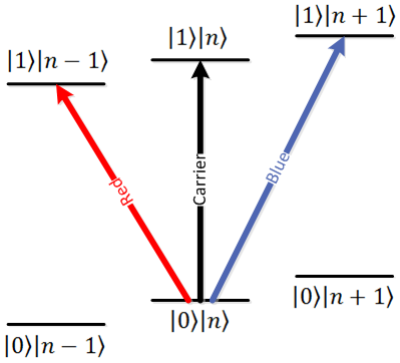

Figure 4: Schematic of vibrational transitions coupled with the electronic-level transitions in trapped ions. The blue sideband adds a phonon and the red sideband takes away a phonon while exciting the internal state. The carrier resonance only excites the electronic level.

Two ions is a common trap potential are coupled by their vibrational modes. Using the blue or red sideband transition laser frequencies, both ions can be excited or decayed into new vibrational states. Using this mechanism two ions can be entangled as follows. The internal ground state of two-ions in the standard basis is $|00\rangle$. When the exciting laser is tuned to the blue sideband for these two ions, they are coupled through the vibrational mode

transition $|n\rangle \rightarrow |n+1\rangle$. If a $\pi/2$ blue laser is applied to the first ion, then only the first ion will get excited with probability $\frac{1}{2}$, and the resulting state is $\frac{1}{\sqrt{2}}(|00\rangle|n\rangle + |10\rangle|n+1\rangle)$. Subsequently, if a red-π pulse then interacts with the second ion, a phonon will be taken away from the system, leaving two qubits entangled in the state will be $\frac{1}{\sqrt{2}}(|00\rangle|n\rangle + |11\rangle|n\rangle)$.

These sideband transitions form the basis of the Cirac-Zoller CNOT gate [26]. In Cirac-Zoller gate, the quantum information of one ion is swapped to the common motional degree of freedom of the ion string. After that, an operation conditioned on the motional state is carried out on a second ion before the quantum information is swapped back from the motional state to the ion internal state. The Cirac-Zoller gate requires ions to be in motional ground states and to be individually addressable.

In another type of implementation of the two-qubit gate called the Molmer-Sorensen gate [35], both ions are illuminated simultaneously. An important advantage of this gate is that the ion string only needs to be cooled into the Lamb-Dicke limit not totally to the ground motional state. As opposed to the Cirac-Zoller gate, the Molmer-Sorensen gate does not require individually addressing the ions. In this scheme the lasers are tuned close to the motional sidebands in such a way that the sum of the frequencies is twice of the frequency of the qubit transition. If we consider two ions in ground states of spin $|0_1 0_2\rangle$ which are coupled through a vibrational mode at frequency ν_m. Applying two laser beams with the beatnotes detuned to the red and blue sides of the carrier frequency $\nu_- = \nu_0 - \mu$ and $\nu_+ = \nu_0 + \mu$, the ions can either absorb first ν_- and then ν_+ or vice versa. Since the total frequency is equal to $2\nu_0$ the state transition $|0_1 0_2\rangle \rightarrow |1_1 1_2\rangle$ occurs. If the beatnote detuning μ is kept sufficiently far from any normal mode frequency then direct vibrational mode excitation can be suppressed. An experiment using the Molmer-Sorenson scheme demonstrated four-ion entanglement in 2000 [28]. Both the Cirac-Zoller and Molmer-Sorenson gates require the laser is tuned near the red or blue sidebands. Well-defined vibration sidebands require that the period of the gate be longer than the vibrational period. As a result the trap frequency puts an upper bound on the gate speed.

2.4.4 Quantum simulation experiments

Since the mid-1990s, several schemes have been proposed for quantum simulation using trapped ions. Some of these schemes have resulted in successful quantum simulation experiments [20]. Pioneering work on trapped-ion analog quantum simulation originated in an experiment using a trapped $^9Be^+$ ion [36]. This work demonstrated that coherent stimulated-Raman pulses can be used to simulate a wide variety of interacting spin-1/2 Hamiltonian systems.

Porras and Cirac were the first to propose that a trapped ion linear chain can undergo a magnetic spin phase transition [37]. Laser beams tuned near the vibrational sidebands of the ion qubit transition can couple the ions in the chain as modeled by an Ising Hamiltonian,

$$H = \sum_{i=1}^{N} \sum_{j=1}^{i-1} J_{i,j} \hat{\sigma^i}_x \hat{\sigma^j}_x + B \sum_{i=1}^{N} \hat{\sigma^i}_y \, . \tag{5}$$

The first term characterizes the spin-spin interactions along the ion chain, where $J_{i,j}$ is the Ising coupling between the spins i and j. The second term characterizes the interaction of each spin with an effective transverse magnetic field B. Following Porras and Cirac's proposal, the first experiment demonstrating the magnetic spin phase transition was performed in 2008 [38]. This experiment used only two $^{25}Mg^+$ ions to demonstrate a weak paramagnetic to ferromagnetic phase transition. This experiment utilized two perpendicularly polarized laser beams to induce state-dependent differential Stark shifts resulting in an optical-dipole force. This force conditionally changes the distance between neighboring spins unless all the spins are aligned in the same direction. The distance between neighboring spins sets simulates the strength of the spin-spin interactions. The effective magnetic field was simulated by applying the RF field tuned to the qubit resonance, equivalent to a qubit rotation. By initializing the ions in the paramagnetic state, tuning the ratio of the first and second terms in (5), the phase of the spin chain system was shown to transition to a ferromagnetic state (i.e. the two spins aligned due to their effective spin-spin interaction) with 88% fidelity.

A series of quantum simulation experiments using linear chains of $^{171}Yb^+$ ions has been

conducted by the Monroe group at UMD [39, 40, 21]. The hyperfine states of $^{171}Yb^{+}$ act as a spin-1/2 system. The spins are optically pumped to the ground states. The spin-state can be detected through state-dependent fluorescence for each ion in the linear chain. In these experiments, the spin-spin interactions ($J_{i,j}$) are achieved by Raman lasers tuned precisely so that difference of frequency is near the motional sidebands associated with the radial phonon modes of the ion chain. In one experiment, K. Kim et. al. [40] studied the spin-frustrations caused by competing anti-ferromagnetic interactions. They observed that the frustration in three-ion chains induced extra degeneracy as the Ising-couplings were adiabatically varied. They also measured the entanglement in the system, finding a link between frustration and ground-state entanglement. In another experiment, R. Islam et al. [21] were able to demonstrate a sharp-phase transition crossover from paramagnetism to ferromagnetic order in a system of nine trapped $^{171}Yb^{+}$ ions. This scheme employed the spin-spin interaction based on Molmer-Sorenson gate to excite the vibrational modes off-resonantly. In this experiment the transversal magnetic field is changed adiabatically and as a result the system follows the instantaneous eigenstates of the changing Hamiltonian. As the system is scaled up to nine ions, the transition of paramgnetism-ferromagnetic order sharpens.

All of the above quantum simulation experiments were performed following the analog approach. Typically a condensed matter quantum system is mapped into the Hamiltonian of a linear-chain of ions. A recent experiment used the digital approach of a universal digital quantum simulator [41]. Using a linear chain of six $^{40}Ca^{+}$ trapped ions, up to 100 gates were performed to fully simulate the dynamics of a range of spin-systems. The system dynamics were explored in these experiments using a stroboscopic sequence of single-qubit and two-qubit gate operations.

The experiments discussed here were performed on linear ion chains and are good examples of how an AQS and DQS can be implemented using linear chains of trapped ions. Since a wide variety of Hamiltonians can be implemented in ion-chain experiments, there

is strong interest in being able to trap stable long chains to perform interesting quantum simulation experiments. According to one estimate, a quantum simulation experiment on 40-ion chain can outperform the classical computer in accurately simulating the quantum behavior of the system [22].

As a benchmark for a successful quantum simulation demonstration that is comparable to the state-of-the art classical computation, a complete description of state and dynamics of a 20-ion chain would stress the capabilities of present day classical computer. A complete description of a 50-ion chain is beyond the capabilities of present day classical computers. The primary goal of this thesis research is to demonstrate trapping of an ion chain consisting of 20 to 50 ions, enabling the demonstration of a quantum simulation that can not be done classically.

CHAPTER 3

ION TRAPS

3.1 Introduction

Trapping charged particles (atomic and molecular ions) has been useful for spectroscopy, mass spectrometry, and quantum state engineering experiments for more than fifty years [42]. As compared to neutral atomic traps, ion traps can rely solely on schemes based on electromagnetic fields. Three factors are to be considered critical in trapping ions: (1) the motional spectrum of the trapped particle, (2) the temperature control, requiring thermal isolation of the particle from environment, and (3) the storage lifetime. Depending upon the application, some factors are more important than the others. For QIP the trapped ions must be cold, occupying only the lower motional states, isolated from the environment in ultra high vacuum, and stored for a long time, long compared to the time required for error-free quantum operations to be performed. Storage times greater than one minute are typically required for quantum simulations. There are four major types of the ion traps:

- **Kingdon Trap**: This trap, originally proposed in 1923 by Kingdon [43], uses only electrostatic force to trap the charged particles. A straight conducting wire at a fixed potential produces a cylindrically symmetric electrostatic potential field. This field scales down logarithmically with the distance from the wire. The charged particles orbit around the wire radially and oscillate axially between end plates to conserve the angular momentum. Since the initial momentum required for trapping of the ions is transferred into the orbital momentum, only hot ions can be trapped using Kingdon trap.

- **Magnetic Bottle Trap**: Orbiting charged particles can be trapped through the Lorentz force created by a variable magnetic field. In a bottle, ions will be trapped radially if the magnetic field varies adiabatically in space from being stronger at the ends to

weaker in the center. Axially an adiabatic invariant parameter can act conditional to the variance in the field, keeping the particle in place [44]. Magnetic bottles cannot confine cold ions since the variation in the Lorentz force causes some orbiting of the trapped ions. This motion will keep ions from being cold, thus, the bottle cannot be used for the gates discussed in Chapter 2. Also the magnetic fields can couple with internal states of ions causing unwanted decoherencefor quantum operations.

- **Penning Trap**: The Penning trap was originally invented by H.G. Dehmelt based on the ideas of F. M. Penning [45] via the invention of the cold cathode high vacuum ionization gauge. The trap uses a uniform magnetic field in the radial plane and the electric field varying quadratically in axial plane. This varying field creates a quadrupole in the axial direction which has a radial anti-confining component and is compensated by a radially uniform magnetic field. By Earnshaw's theorem this compensation creates a saddle for ion to be confined. Ions can be cooled in a Penning trap which makes it useful for QIP. The major problem is controlling the uniformity of magnetic fields. Any field variation cannot only cause excessive cyclotron motion, but also unwanted Zeeman splittings in internal states of the ions. In Penning traps it is possible to form a triangular-shaped 2D lattice or Wigner ion crystals that can be used to simulate spin-spin coupling. The ion spacing is large enough that the ions can be addressed individually by laser beams [37].

- **Paul Trap**: This trap was invented by W. Paul in 1953. In addition to mass spectrometry and spectroscopy applications, Paul traps are also used in QIP field. Paul traps confine ions in three dimensions. They use a combination of electrostatic and time-varying electric fields and require very small ion motion compensation potentials. For this reason Paul traps are favored for storing ions that can be cooled to ground state and require very small ion motions for confinment. Ion storage times

with laser cooling can be as long as many days, long enough for even the most ambitious quantum processing algorithm. The theory of the confinement of an ion in the Paul trap is discussed in details in the following section.

3.2 Paul trap confinement principles

To trap a particle, restoring force on the particle has to be proportional to the negative of the distance from the origin of the trap, $F \propto -r$. Both Paul and Penning traps create such a force through a quadrupole potential Φ, which in three dimensions can be written as

$$\Phi = \frac{\phi_0}{r_0^2}(\alpha x^2 + \beta y^2 + \gamma z^2), \tag{6}$$

where ϕ_0 denotes a voltage applied to a quadrupole electrode configuration, r_0^2 is the characteristic trap size, and the constants α, β, γ, determine the shape of the potential [46]. Solving the Laplace equation $\nabla^2\Phi = 0$ requires $\alpha + \beta + \gamma = 0$. The three-dimensional quadrupole potential is described by $\alpha = \beta = -2\gamma$, and a two dimensional quadrupole potential by $\alpha = -\beta, \gamma = 0$. The different signs of the factors α, β, γ, make it evident that stable confinement cannot be achieved with a purely static electric potential. A time-dependent potential, $\phi_0 = V_{dc} + V_{ac}\cos(\Omega_{RF}t)$, can be applied in the transverse directions (x and y in Figure 5) to achieve a stable confinement. The time-varying potential is achieved by applying a radio-frequency (RF) electric field. This configuration is known as the Paul trap in three dimensions and the Paul mass filter (linear trap) in two dimensions. The linear trap provides a radial binding force along the z-axis (See Figure 5) that is used to guide ion beams for mass spectrometry. Three-dimensional traps provide a confining force with respect to a single point in space and are therefore used for single-ion experiments or for the confinement of large symmetric ion clouds.

A linear version of the Paul trap can be realized by four conducting rods as shown in Figure 5. Two opposing rods are connected to one pole of a RF voltage source (dark electrodes in Figure 5,) whereas the remaining two rods are connected to the other pole. The axis of symmetry between the rods is the axis of trap. The opposite polarities of two

sets of rods push and pull ions. Since these polarities are generated using rapid time-varying RF field, the effective force pushes the ion toward center where it becomes trapped. To confine the ions' motion in the axis parallel to trap axis, DC potentials are generally added to a pair of conductors (white rods in Figure 5) [47].

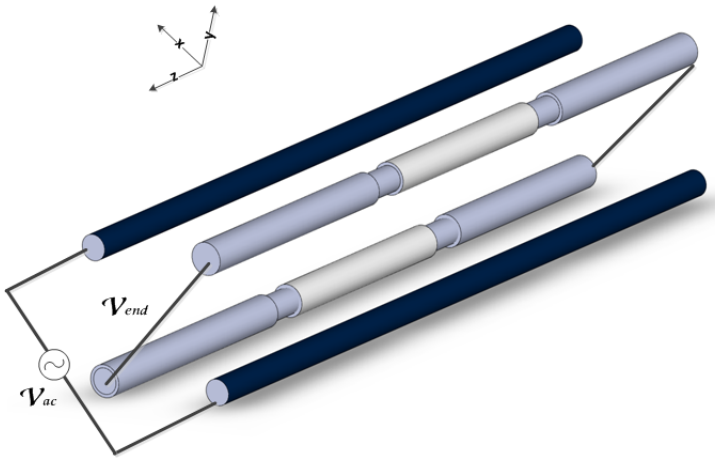

Figure 5: Schematic drawing for linear RF trap. Dark electrodes have common RF potential, grey and white rods have dc potentials.

By applying superimposed dc and rf potentials, $\phi_0 = V_{dc} + V_{ac}\cos(\Omega_{RF}t)$, the quadrupole radial potential becomes

$$\Phi(t, x, y) = \left(\frac{V_{dc} + V_{ac}\cos(\Omega_{RF}t)}{2r_0^2}\right)(x^2 - y^2), \tag{7}$$

where r_0 is distance from the rod surface to the trap center. An electrostatic potential V_{end} is applied axially to confine ion in that direction, adding an axial quadrupole potential. The radial dependence of this potential follows from Laplace's equation. If the trap is assumed to be symmetric in x- and y-direction

$$\Phi_{ax}(x, y, z) = \left(\frac{\kappa V_{end}}{d_0^2}\right)\left(z^2 - \frac{x^2 + y^2}{2}\right), \tag{8}$$

where d_0 is distance from the trap center to the electrode in axial direction and κ is trap geometrical parameter that can be found experimentally. The total radial quadrupole is

then

$$\Phi_r(t,x,y) = \left(\frac{V_{dc} + V_{ac}\cos(\Omega_{RF}t)}{2r_0^2} - \frac{\kappa V_{end}}{2d_0^2}\right)x^2 + \left(\frac{-V_{dc} - V_{ac}\cos(\Omega_{RF}t)}{2r_0^2} - \frac{\kappa V_{end}}{2d_0^2}\right)y^2. \quad (9)$$

The equation of ion motion can now be derived from the radial potential given in (9). Assuming that the motions of the ion in the x- and y-direction are not coupled, then $-e\frac{d}{du}(\phi_r(t,u)) = m\ddot{u}$ where $u = x$ or y and e is charge of electron and m is mass of an ion. This leads to

$$\begin{aligned} \ddot{x} + \frac{e}{m}\left[\frac{V_{dc} + V_{ac}\cos(\Omega_{RF}t)}{r_0^2} - \frac{\kappa V_{end}}{d_0^2}\right]x(t) = 0 \\ \ddot{y} + \frac{e}{m}\left[\frac{-V_{dc} - V_{ac}\cos(\Omega_{RF}t)}{r_0^2} - \frac{\kappa V_{end}}{d_0^2}\right]y(t) = 0. \end{aligned} \quad (10)$$

The system of equations in (10) can be written in the form of Mathieu's equations with $\Omega_{RF}t = 2\tau$,

$$\begin{aligned} x(\ddot{\tau}) + (a_x + 2q_x\cos 2\tau)\,x(\tau) = 0 \\ y(\ddot{\tau}) + (a_y + 2q_y\cos 2\tau)\,y(\tau) = 0\,, \end{aligned} \quad (11)$$

where,

$$\begin{aligned} a_x &= \frac{4e}{m\Omega_{RF}^2 r_0^2}\left[V_{dc} - \frac{r_0^2\kappa V_{end}}{d_0^2}\right] \\ a_y &= \frac{4e}{m\Omega_{RF}^2 r_0^2}\left[-V_{dc} - \frac{r_0^2\kappa V_{end}}{d_0^2}\right] \\ q_x &= -q_y = \frac{2eV_{ac}}{m\Omega_{RF}^2 r_0^2}\,. \end{aligned} \quad (12)$$

The solution of the Mathieu's equations describes the ion motion in a linear Paul trap with three frequencies of harmonic motion $\omega_x, \omega_y, \omega_z$. This motion is referred to as *secular* motion. For the case $V_{dc} \cong 0$, $a_x = a_y$, and $a_x \ll q_x^2 \ll 1$ the approximate solutions to (11) is given as [47],

$$\begin{aligned} x(t) &= x_0\cos(\omega_x t + \varphi_x)\left(1 + \frac{q_x}{2}\cos\Omega_{RF}t\right) \\ y(t) &= y_0\cos(\omega_y t + \varphi_y)\left(1 + \frac{q_y}{2}\cos\Omega_{RF}t\right), \end{aligned} \quad (13)$$

where $x_0,\ y_0,\ \varphi_x,\ \varphi_y$ are determined by in initial conditions and $\omega_x = \frac{\Omega_{RF}}{2}\sqrt{\frac{q_x^2}{2} + a_x}$ and $\omega_y = \frac{\Omega_{RF}}{2}\sqrt{\frac{q_y^2}{2} + a_y}$ are secular frequencies. The amplitude of this secular motion is weakly modulated at the driving frequency Ω_{RF}. This weak modulation is known as *intrinsic micromotion*. Intrinsic micromotion is typically very small compared to the secular motion and negligible for most QIP cases. For ideal Paul traps, the quantum motion of a single ion located near the trap center is very well approximated by a harmonic oscillation in three dimensions.

The parameters a_x, a_y, q_x, and q_y in the system of equations (11) are unit-less and referred as stability parameters. The a_x and a_y parameters describe the "stiffness" of the trap while q_x and q_y describe the "excitation" of the trap. These parameters play an important role in determining the operating conditions of the trap. In mass spectrometry these parameters are used to filter out the undesirable masses or, by measuring these parameters, the masses are identified. In the applications of ion traps for QIP, the a, q parameters are selected to be small enough (typically $a < 0.1$ and $q < 0.5$) so that the ion remains in the primary stability region of the trap and the adiabatic approximation remains valid. For a charged particle in high-frequency field confinement, the effective potential can be approximated by the mean kinetic energy of the ion oscillation. This implies the assumption that the total kinetic energy remains constant while the ion is fluctuating between high frequency oscillations and slower average motion. Due to this approximation, the *adiabaticity parameter* β_x^{ad} can be approximated by $\beta_x^{ad} \approx a_x + \frac{q_x^2}{2}$. The ratio of the exact value of β_x and β_x^{ad} remains close to 1 only for $a_x \ll q_x \ll 1$. This approximation is also referred to as "pseudopotential approximation."

3.3 Laser cooling

In an ion-trapping experiment, ions are produced either by laser ablation or by heating an atomic source to evaporate neutral atoms and a photo-ionization process. In the laser ablation process a high-intensity laser is focused on the atomic source causing the rapid

ejection of atoms, ions, molecules, and electrons. A more popular technique is to use an oven that can be heated until the atomic source material starts to evaporate neutral atoms. The neutral atoms are ionized using a laser beam at a neutral resonance and a second ionizing laser beam. Depending upon the temperature of the source and the energy added by electric fields, the ions can have energies on the order of an electron volt (eV) [48]. For quantum computing with trapped ions, the ions have to be cooled to the lowest possible motional state. Especially for the Cirac-Zoller gate scheme, the ion has to be cooled down to its motional ground state.

Cooling the trapped ions using lasers utilizes the Doppler effect. During the interaction between lasers and ions, the ion will see the actual laser frequency (ω_0) only if the ion is at rest. If the ion is moving into the laser field with velocity $\mathbf{v}$, then the frequency in the ion's frame of reference, $\omega_+ = \omega_0 + \mathbf{kv}$. If the ion is moving away from the laser field then the frequency will be Doppler-shifted to $\omega_- = \omega_0 - \mathbf{kv}$. The ions' absorption spectrum is broadened by these Doppler shifts. This Doppler shift mechanism is used to cool the ion since momentum is transfered at each absorption event. The laser is detuned to the low side of the absorbing resonance so that the ions see a positive Doppler shift and absorb momentum from the laser photons. The detuned frequency is less than the resonant frequency $\omega_- = \omega_0 - \delta$, where δ is the detuning. This absorption is followed by spontaneous emission in a random direction and the ion emits a photon with frequency ω_0 and loses momentum and energy. This absorption-emission cycle occurs several times, as the ion loses more energy and cools down. For a hot ion, the Doppler-broadened emission linewidth is much larger than the linewidth of the laser. With the laser detuned below the resonance, the probability of emitting a photon with higher energy is higher than the the probability of emitting a photon with the input energy.

There is a fundamental limit to the Doppler cooling process. It arises from the conservation of momentum. When an ion spontaneously emits a photon in a random direction it recoils. Even though the random recoils are small and cancel out on average, they limit

the cooling effect. The minimum temperature (T_{min}) that can be achieved by the Doppler cooling is a function of the transition lifetime, τ,

$$T_{min} = \frac{\hbar}{2k_B\tau}, \tag{14}$$

where k_B is Boltzman's constant. Doppler cooling typically results in a motional state of the ion between $|n = 10\rangle$ to $|n = 30\rangle$ for the axial frequencies near a megahertz [49].

For the ion $^{40}Ca^+$ the cooling transition energy-level scheme is shown in Figure 6. For $^{40}Ca^+$, the cooling transition $4^2S_{1/2} \leftrightarrow 4^2P_{1/2}$ is at a wavelength of 397 nm. The lifetime of $4^2P_{1/2}$ state decaying to the $4^2S_{1/2}$ state is 10 ns. Selection rules also allow ion decay from $4^2P_{1/2}$ to the $3^2D_{1/2}$ state. The decay rates can be calculated using Clebsch-Gordon coefficients. The ratio of the decay rates of two transitions is approximately $1/15$ [49]. Since the $3^2D_{1/2}$ is a meta-stable state with a lifetime of 1 s, it is essential to incorporate a repumping beam with a wavelength of 866 nm, for the $4^2P_{1/2} \leftrightarrow 3^2D_{1/2}$ transition.

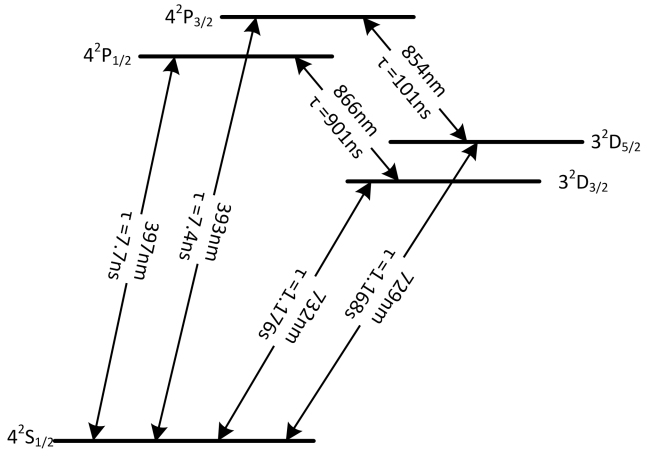

Figure 6: ^{40}Ca cooling transition of the 397 nm and repumping 866 nm transition.

Quantum gates and quantum simulations require the ion to be cooled-down to near the motional ground state $|n = 0\rangle$. To cool the ion lower than Doppler limit, T_{min}, additional laser cooling techniques can be used. One of the techniques that is typically used for $^{40}Ca^+$ ion is called *sideband cooling*. For a trapped ion, the internal level for the $4^2S_{1/2}$ to $3^2D_{5/2}$ transition (often used as an "optical qubit",) is coupled to external motional levels. When the ion is Doppler cooled to roughly T_{min}, which is $\sim mK$ for $^{40}Ca^+$, the vibrational

sidebands of its internal transition are resolved into sidebands with frequency splitting in the MHz range. The sideband cooling cycle is shown in Figure 7. Laser pumping of selected vibrational sidebands can be used to bring the ion to its vibrational ground state, $|n = 0\rangle$. The ion can be cycled through this transition repeatedly until it is in the ground state. To make this cycling work the ion has to be brought back to the $|0\rangle$ internal state. When the ion is excited from $|0\rangle|n\rangle$, it either decays back to one of the three states, $|0\rangle|n\rangle$, $|0\rangle|n-1\rangle$, or $|0\rangle|n-2\rangle$ (See Figure 7, right side). The combined probability of $|1\rangle|n-1\rangle \rightarrow |0\rangle|n-1\rangle$ and $|1\rangle|n-1\rangle \rightarrow |0\rangle|n-2\rangle$ transitions is more than the probability of transition back to initial state. On average, the ion will loose vibrational energy cycling through these transitions.

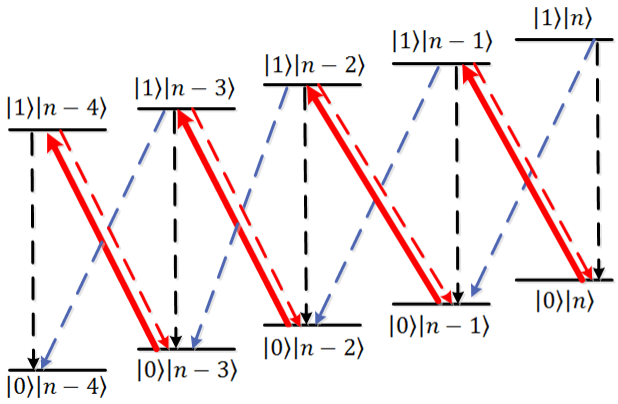

Figure 7: Generic mechanism of sideband cooling. The ground $4^2S_{1/2}$ state is denoted by $|0\rangle$ and the excited $3^2D_{5/2}$ state by $|1\rangle$.

For $^{40}Ca^+$ the $4^2S_{1/2} \leftrightarrow 3^2D_{5/2}$ transition is at a wavelength of 729 nm. The $3^2D_{5/2}$ state has lifetime of 1 s, resulting in a slow cooling rate. If another transition, the $3^2D_{5/2} \leftrightarrow 4^2P_{3/2}$, is brought into play the ion can decay back into $4^2S_{1/2}$ faster. Typically, using this cycle the $^{40}Ca^+$ ion can be brought to the vibrational ground state in few tens of milliseconds [49].

3.4 Linear trap geometries

The linear Paul trap has found applications in biology, chemistry, and physics primarily as a mass spectrometer. Paul traps have been commercialized and are being used to analyze

gases, distinguish isotopes, trace drugs and pollutants, and detect volatile organic species. With this demand, the need to miniaturize the device has arisen. Several miniaturized traps have been demonstrated that are made using technologies ranging from micro-machining to micro-fabrication with standard Si based technology [42, 50]. Miniaturization is motivated not only due to the interest in the size reduction enabling portability, but also due to the interest in operating conditions which are only possible in traps with smaller-dimensions. Since the trap geometry parameters r_0 and d_0 described in Section 3.2 can have a direct effect on the voltage ranges and RF frequencies applied to the trap, the smaller traps have higher signal to noise ratios, enabling their application in high-pressure mass spectrometry [42, 51]. Additionally, mass spectrometers based on arrays of miniaturized traps are useful in lab-on-chip applications.

In QIP, with the successful demonstrations of eight-qubit entanglement, long chains, and proposals to do large-scale quantum computations with the trapped-ions platform [52], miniaturization is an area of active research in the scientific community [53]. Similar to the mass-spectrometer case, the smaller traps in QIP are expected to control more and more ions that can be manipulated by the lasers or microwaves for performing logical operations. In other words, there is strong interest in making traps ”scalable” so that they can handle more ions. Proposals for applications based on scalable traps include the trap arrays, junctions that utilize the ion-transportation, traps that are small enough to handle 1D chains with small inter-ion spacing, traps that have integrated optical elements such as mirrors, Fresnel lenses, fiber-optic tips, and the traps that have multiple trapping zones with assigned functionalities such as ion-storage, computing, and read-out zones. This interest in the ion-trap miniaturization has been advanced by

1. the development of the geometries and designs that can utilize the micro-machining and micro- or nano-fabrication technologies,

2. advancements in the instrumentation, vacuums, and fabrication technologies.

Several geometries and versions of the miniaturized linear trap have been designed and demonstrated with the promise of QIP with scalable trapped ions. These traps are made either with the micro-machining tools or with the microfabrication technologies. Following the design of the four-rod linear trap (Figure 5), the linear trap requires RF electrodes to form a radial quadrupole potential and DC electrodes for electrostatic axial quadrupole confinement. The designs can be categorized into three classes depending upon how the RF and DC (control) electrodes are configured, i.e., two-level, three-level, and surface-electrode traps.

3.4.1 Two-level traps

One straightforward way to make a four-rod trap smaller is to translate the rods into flat electrodes bonded to a structure so that it mimics the alternating rod configuration of standard four-rod trap. Geometries demonstrated in [54] and [55] are the earliest demonstrations of the two-level linear trap. The trap dimensions are in the hundreds of microns. These traps were built with micro-machining tools. The two-level geometry from [55] is shown in Figure 8(a) as an example. Compared with the four-rod geometry shown in Figure 5, the alternating rods are mapped to alternating RF plates and DC rods to metal plates which are electrically insulated from the RF plates. These flat plates could be very thin sheets of metal or insulators coated with metal sheets.

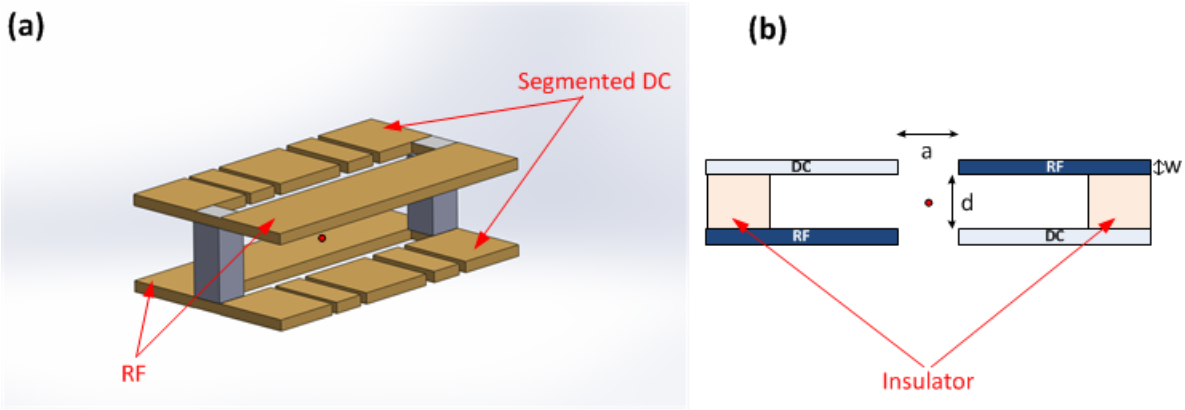

Figure 8: A two-level linear ion trap example geometry from [55] is reproduced in (a) and simplified version is shown in (b).

A schematic drawing of the two-level geometry is shown in Figure 8(b). This trap creates a symmetric radial field where the quadrupole field and its gradient are the same in the radial dimensions. This geometry results in a higher trapping depth as compared with the planar traps of similar dimensions. The secular frequencies of the two-level traps are comparable to the four-rod traps of similar dimensions. Two-level traps have the advantage of superior trapping characteristics as compared to other kinds of the miniaturized traps, but due to the geometric constraints, the fabrication is more difficult. The smallest two-level traps that have been built to date have dimensions on the order of hundreds of microns. These traps are typically not made with a single substrate nor are they monolithic. Some recent examples of the two-level traps are given in [53, 56, 57, 58].

As discussed in [56], three parameters considered in designing of a two-level trap are:

- A geometric efficiency parameter (η), which fixes the deviation of quadrupole from being harmonic is the ratio of potential created by linear geometry and the potential created by hyperbolic (ideal) geometry $\eta = \frac{\Phi_{LMT}}{\Phi_{Hyp}}$.
- The aspect ratio (α) is the ratio of horizontal and vertical separations of the two rods, as shown in Figure 8(b), $\alpha = \frac{a}{d}$. In [56], the authors investigated the relation of the aspect ratio and efficiency and found that the efficiency decreases with increasing the aspect ratio till it asymptotically reaches $1/\pi$ for two-level designs.
- The ratio of the electrode thickness and the separation of two electrodes on one side $\delta = \frac{d}{t}$.

In addition to these factors there are several other considerations which are to be made in designing the ion trap. Some of them will be discussed in Section 3.5.

3.4.2 Three-level traps

From the linear trap four-rod geometry, the ponderomotive potential can be mapped into a geometry with three levels of electrodes. RF and DC assignments can be made to alternating electrodes vertically as shown in Figure 9. In Figure 9(a) and Figure 9(b) two different

configurations of simplified three-level geometries are shown. The configuration shown in Figure 9(a) was proposed to be used as a quantum charged couple device (QCCD) [52]. These geometries consist of the conducting electrodes separated vertically by the insulating material.

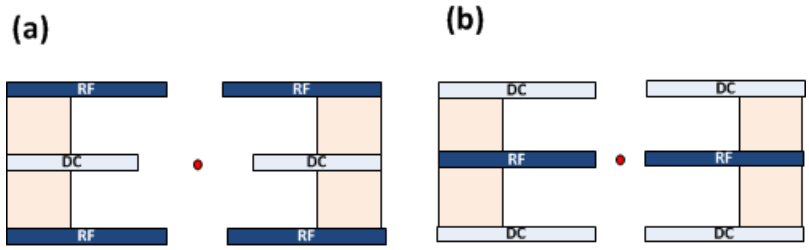

Figure 9: Schematic drawings of simplified three-level trap geometries.

The three-level geometries shown in Figure 9 produce symmetric harmonic radial confinement. Like two-level geometries, three-level traps have deeper trapping depths as compared with the four-rod traps of same size and have larger secular frequencies. Compared to the two-level geometries, three-level traps allow more control of the ion position and the use of complicated geometries such as junctions and multi-zone trap arrays. Three-level geometries, however, are more demanding from fabrication standpoint. The design guidelines for these traps follow same constraints on the parameters, α, η, δ as described in previous section. These parameters have to be carefully optimized along with the other requirements based on the particular QIP experiment of interest.

A numerical study of the three-level trap strength (trapping depth) and its parameters [59] suggests that the thickness of the insulating layer between electrodes should be an order of magnitude thicker than the thickness of the electrodes. This requirement adds challenges in fabricating three-level traps, since conformal etching of the low-loss insulating materials is difficult. Because of the three-level trap's thick insulating layer requirement, it is challenging to have sufficient optical-access and yet have reasonable aspect ratio (α).

3.4.3 Surface-electrode traps

Two- and three-level traps have the advantages of being symmetric and having deeper potentials; however, they face the severe fabrication challenges. Planar surface-electrode traps have been more popular for arrays and scalable configurations because they are easier to fabricate. The concept of the linear trap can easily be adopted to construct surface-electrode-planar traps. A straightforward way to modify the 3D design of Figure 5 is to place four "rods" in a common plane and trap the ion above the surface with alternating RF and control electrodes as shown in Figure 10. A four-wire surface-electrode ion trap is shown in Figure 10(a). A five-wire geometry, with inherent mirror symmetry that can be useful in controlling the trap axes, is shown in Figure 10(b). The four-wire geometry, shown in Figure 10(a), has a radially asymmetric potential because the DC-electrodes are not segmented on both sides. This asymmetry can couple the trapped ion motion in the two radial directions as discussed in detail in Chapter 4. Static potentials applied to the control electrodes of surface-electrode trap produce radial "trapping" and "anti-trapping" components to fields at the ion site that define the trap principal axes. In the four-wire planar trap geometry, the principal axes are rotated and are at 45° to the plane, while in the five-wire geometry the principal axes are perpendicular and parallel to the plane. The principal axes not being at an angle to the plane can reduce laser-cooling efficiency. For an ion to be cooled efficiently, all the axes have to be at some angle to the wavevector of the cooling laser. Since, for surface traps the laser-access is typically parallel to the plane, rotating the ion's principal axes is desirable. The five-wire geometry can be modified to have asymmetric RF rail widths providing the required the principal axes rotation.

Surface-electrode traps have the flexibility of altering the geometry to vary the trapping depth and location of the ions. This results in more control over the confinement of multiple ions. Multiple ions can be manipulated by varying the control potentials near the trapping region. In the five-wire geometry the central electrode can be segmented for that purpose [59]. A major advantage of the surface-electrode designs is that they can

easily be miniaturized using microfabrication techniques. Because of this flexibility, these traps can be designed and scaled up for multi-qubit systems. Several refesearch groups have been interested in exploring different microfabricated surface-electrode trap designs for QIP applications [53, 59]. Although, microfabrication technologies are not limited to planar surface-electrode traps, their application to surface-electrode traps allow designs for a variety of large scale processing schemes such as transporting of ions through different zones using junctions and integration of optics components into trapping regions. A detailed review of current microfabricated traps for QIP can be found in [53].

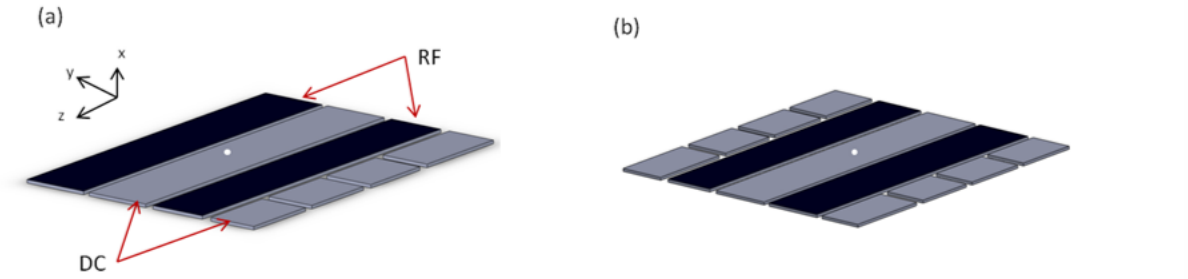

Figure 10: Two surface-electrode geometries are shown. All electrodes are in a plane. In (a) the four-wire geometry of surface-electrode trap is shown and in (b) the five-wire version of surface-electrode trap is shown.

Design of the planar electrodes can be achieved using conformal mapping [60]. Conformal mapping is used to map a two-dimensional problem to a problem in the complex plane. The solution of the Laplace equation in the region of the electrodes can be mapped from ($\nabla^2\Phi(\mathbf{r}) = 0$) to another solution ($\nabla^2\Phi(\mathbf{M}(\mathbf{r})) = 0$), where $\mathbf{M}(\mathbf{r})$ is a conformal map, if and only if $\mathbf{M}(\mathbf{r})$ is analytical. This tool can be utilized to solve the problem of determining surface-electrode dimensions that will create a quadrupole of the desired strength and orientation. We use a conformal map to a symmetric cylinder centered at the desired quadrupole null [60].

3.5 Design considerations for microfabricated traps

Miniaturized versions of the traps are primarily interesting for QIP. With the promise of multi-qubit operations the ion traps are to be designed to hold ions in different positions, lattices, and configurations. The design process for microfabricated ion traps is not only driven by this demand for miniaturization but also several other aspects ranging from trapping characteristics and experimental requirements to the ability to fabricate traps using standard (or easily available) technologies. An abstract-level process flow for designing the ion traps for QIP is given in Figure 11.

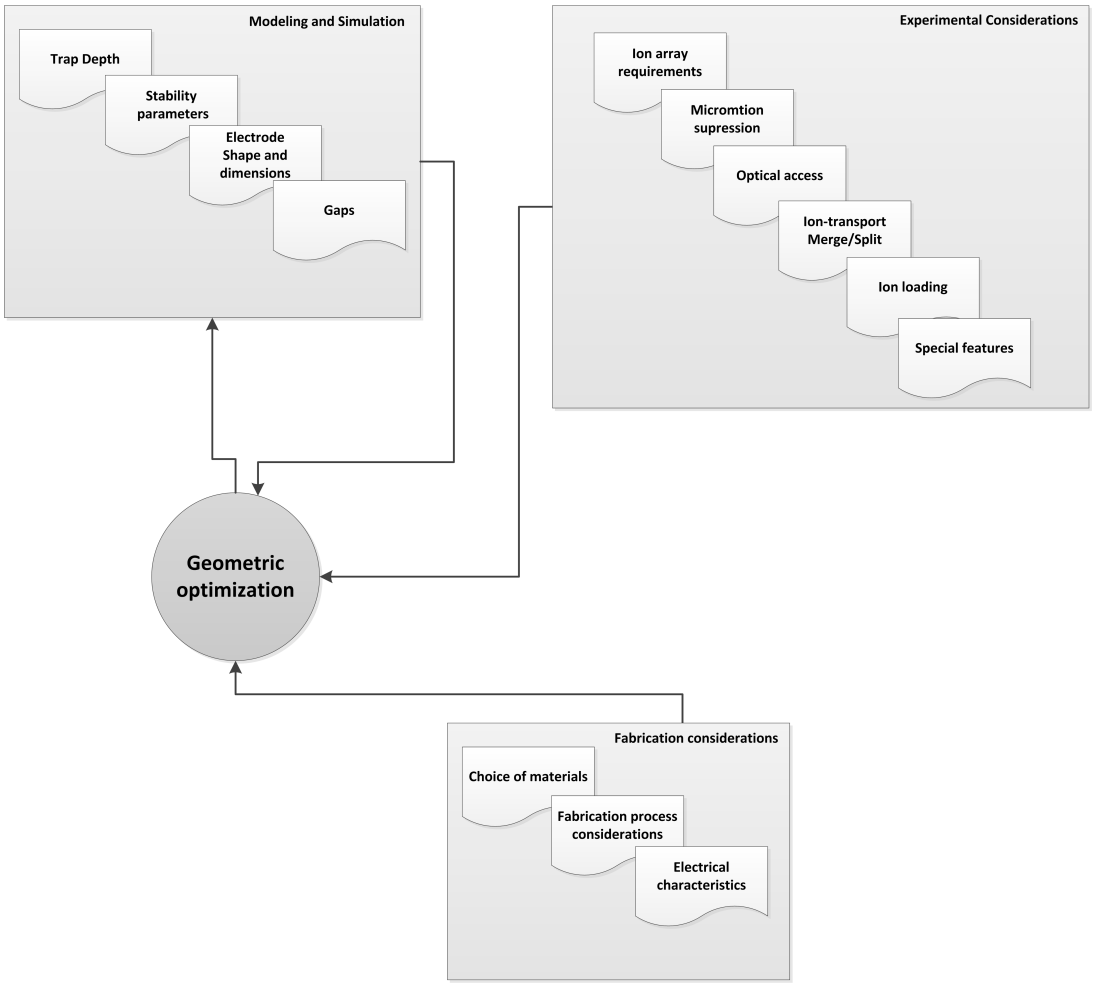

Figure 11: The design process flow for designing the ion traps for QIP experiments.

3.5.1 Trapping characteristics

For QIP experiments some of the trapping characteristics of the ion trap have specific requirements as compared to the other applications. Here the discussion of the design process and the factors that have to be optimized are mainly in the context of microfacricated traps for QIP experiments. Some aspects are specific to the surface-electrode designs; however, some can be generalized to both multi-level and surface-electrode designs.

3.5.1.1 Trap depth

Trapping depth is defined as the minimum energy required for a trapped ion to escape the pseudopotential (See Section 3.2.) Since the ion is trapped at the zero of the electric field (null), the trap depth is a critical parameter to be optimized for stable confinement. Electrodes are not only to be shaped to achieve sufficient trapping depth but also have to have appropriate dimensions. A detailed analytical study of the trapping depth and corresponding planar RF electrode dimensions for surface-electrode traps is found in [61, 60]. Using the pseudopotential approximation (also known as adiabatic approximation or potential-well model), the trap depth can be derived by assuming that the amplitude of the secular motion of an ion is much larger than the amplitude of the intrinsic micromotion, a good assumption in cases of interest. Choosing ion motion along the x-axis and denoting secular motion by x_s and intrinsic micromotion by δx, this assumption requires $x_s \ll \delta x$. Another assumption is that the change in the secular motion with time is relatively small compared with change in the RF-caused micromotion, that is $\frac{d(\delta x)}{dt} \gg \frac{dx_S}{dt}$. The total ion motion in the x-direction is the sum of two motions, $X = x_s + \delta x$. Following the procedure in [46] and using $2\tau = \Omega_{RF} t$,

$$\frac{d^2 x_s}{d\tau^2} = -\frac{(\beta_x^{ad})^2 \Omega_{RF}^2 x_s}{4} = -\frac{e^2 V_{ac} x_s}{2m^2 \Omega_{RF}^2 r_0^4},$$

where $\beta_x^{ad} \approx a_x + \frac{q_x^2}{2}$, $a_x \sim 0$, and q_x from (12) in Section 3.2 is used. Using the equation of motion for a charged particle in a parabolic pseudopotential (ϕ_x),

$$m\frac{d^2 x_s}{d\tau^2} = -e\frac{d\phi_x}{dx_s},$$

or,

$$\frac{d\phi_x}{dx_s} = -\frac{eV_{ac}x_s}{2m\Omega_{RF}^2 r_0^4},$$

and the depth of the pseudopotential, $\Delta\phi_x$ is,

$$\Delta\phi_x = \int_0^{r_0} \frac{d\phi_x}{dx_s}\,\mathrm{d}x_s = -\frac{eV_{ac}^2}{4m\Omega_{RF}^2 r_0^2}\ .$$

Given a "five-wire" surface-electrode geometry with RF infinite strips of equal widths b, and a central control electrode at ground of width a, the expression for r_0 in terms of a and b [61] is,

$$r_0 = \frac{(a+b)^2 + (a+b)\sqrt{2ab+a^2}}{b}\ . \tag{15}$$

Similarly, using the Mobius transformation given in [60], the dimensions a and b can be written in terms of angles spanned by the arcs describing the electrode dimensions. Using these expressions the trapping dimensions can be optimized to obtain a deeper trap once the geometry is finalized. For two-level traps a similar analysis derived the the trap depth expression in terms of the dimension a and d (Figure 8).

3.5.1.2 Stability parameters

Besides describing the trapping depth, the electrode shape and dimensions have an effect on the stability parameter q_x and q_y (referred to as "excitation" parameters). These q-parameters determine the pseudopotential curvature. Using expressions given in (12) and (15), q can be written as,

$$q = \frac{2eV_{ac}b^2}{m\Omega_{RF}^2\left[(a+b)^2 + (a+b)\sqrt{2ab+a^2}\right]^2}\ .$$

The electrode design can be optimized such that $q \ll 1$. This condition is important for ion stability, the validity of the adiabatic approximation, and the high-order terms of quadrupole to be negligible.

3.5.1.3 Micromotion

In the context of the ion traps, there are two types of micromotion. Intrinsic micromotion is the motion due to RF electric field, where secular motion is modulated at the RF frequency.

The amplitude of the intrinsic micromotion is much less than that of the secular motion in QIP experiments. This is true even for ions cooled to the ground state. Using the expression in (13) the intrinsic micromotion term of the kinetic energy of an ion averaged over a period of secular motion is [62],

$$KE_{in}^{x} = \frac{q_x^2 m x_0^2 \Omega_{RF}^2}{32} .$$

With the laser cooling of secular motion, the amplitude x_0 is reduced.

If there is a stray field at the ion site, caused by any trap electrode imperfection or built-up of charge in the dielectric material used in the trap, the DC quadrupole null and RF quadrupole null are offset. This misalignment causes "extrinsic" micromotion. Extrinsic micromotion can cause multiple problems, e.g., broadening of cooling transition linewidth, second-order Doppler shift, and A.C. Stark-shifts. In designing the traps, great care must be taken so that the sources of extrinsic (excess) micromotion are minimized. If the stray field is $\mathbf{E_s}\hat{x}$ in x-direction, then the equation of motion in x direction is,

$$\ddot{x(\tau)} + (a_x + 2q_x \cos 2\tau)\, x(\tau) = \frac{e}{m}\mathbf{E_s}\hat{x} \,, \tag{16}$$

and the solution of (13) is modified,

$$x(t) = (\Delta x_0 + x_0)\cos(\omega_x t + \varphi_x)\left(1 + \frac{q_x}{2}\cos\Omega_{RF} t\right), \tag{17}$$

where $\Delta x_0 \approx \frac{8e\mathbf{E_s}\hat{x}}{m(2a_x+q_x^2)\Omega_{RF}^2}$ as shown in [62]. The kinetic energy due to the extrinsic micromotion can be written as,

$$KE_{ex}^{x} = \frac{4}{m}\left(\frac{eq_x\mathbf{E_s}\hat{x}}{(2a_x + q_x^2)\Omega_{RF}}\right)^2 . \tag{18}$$

It can be seen that the micromotion is not dependent on the secular motion amplitude x_0; thus, cooling alone will not suppress the motion. External compensation fields have to be applied to minimize $\mathbf{E_s}$. Typically this is done using compensation control electrodes and fields. Segmenting the control electrodes helps in applying the compensation fields. One of the adverse effects of the extrinsic micromotion is due to the accompanying Doppler shift. The Doppler shifts can significantly alter the effective cooling transition linewidth. This

can result in the cooling beam starting to heat the ion if frequency offsets of the cooling laser from the cooling transition line center are not increased. The micromotion amplitude can be deduced from (18),

$$x_{ex} = \frac{1}{2} q_x \Delta x_0 = \frac{4eq_x \mathbf{E_s} \hat{x}}{m(2a_x + q_x^2)\Omega_{RF}^2}. \tag{19}$$

This extrinsic micromotion causes the laser field at the ion to be modulated at the RF frequency, creating sidebands. The intensity of the laser at the carrier frequency is reduced and is distributed among the sidebands. This modulation is parameterized by the modulation index β. For a laser, which has a wavevector with the x-component $\mathbf{k} = \frac{2\pi}{\lambda} \cos\theta$, a wavelength λ, and the angle θ with the direction of micromotion, the modulation index is given by

$$\beta = \mathbf{k} x_{ex} = \frac{8\pi eq_x \mathbf{E_s} \hat{x}}{m\lambda(2a_x + q_x^2)\Omega_{RF}^2} \cos\theta. \tag{20}$$

The modulation index $\beta > 1$ causes on-resonance fluorescence loss. It is desirable to have $\beta < 0.25$. One of the main sources of micromotion is the stray fields produced by dielectric charging. If the scattered laser light strikes the dielectric material that has a line-of-sight to the ion, the charging can cause stray-fields of the order of thousands of V/m sufficient to cause β to increase beyond 0.25.

Since extrinsic micromotion depends on the stability parameters and RF frequency, which are geometry dependent, it is important to consider these parameters during the design phase.

3.5.1.4 Electrode shapes and dimensions

The trapping of the ion in the radial plane is due to the RF pseudopotential well. Axial trapping, on the other hand, is due to fields of the DC (control) electrodes. In order to avoid unnecessary micromotion, it is necessary to choose the control electrode designs and voltages that result in vanishing radial components of the DC field at the ion location. On the other hand, the RF electrodes' asymmetries can cause a phase difference in the applied RF field. This phase difference can cause extra intrinsic micromotion and is analyzed in

details in [62].

Design work at the Quantum Information Systems (QIS) group at Georgia Tech Research Institute (GTRI), incorporates genetic-algorithms (GA) with multi-objective fitness functions to optimize electrode shapes, to minimize ion heating due to pseudopotential deformations (bumps), and to maintain constant secular frequency along the transport path [63]. The work on junctions and linear traps by different groups has explored different electrode shapes to optimize the fields and minimize the pseudopotential bumps. Surface-electrode traps typically have through-substrate slots used to load ions from the back-side of the substrate. The shape of this slot can be optimized to minimize the pseudopotential bump introduced by the slot. The last few generations of the surface-electrode traps designed and fabricated at the QIS lab have applied GA to optimize the RF electrode and loading slot shapes. Similarly, in multi-zone geometries, the pseudopotential transitions between zones can be smoothened by designing the appropriate electrode shapes.

Using the techniques discussed in [61] and the Biot-Savart law applied in [60] on a rectangular electrode, the electrostatic field for a given set of voltages can be obtained by using Green's functions. The line integral formulated for a rectangular electrode set to a non-zero potential while assuming the rest of the plane at zero potential can be written as

$$\mathbf{E}_{\mathbf{x}} = \frac{V}{2\pi} \oint_C \frac{d\acute{s} \times (x - \acute{x})}{|x - \acute{x}|^3} \tag{21}$$

which is same as the formula for the magnetic field of a current on a wire that following electrode boundary. In (21), $d\acute{s}$ is line element along the boundary C of the electrode, and V is the voltage applied. The integral is evaluated in counter-clockwise direction of the normal to electrode plane. This model can be applied to DC electrodes with the assumption that the electrodes are gapless. Although the segmentation of DC electrodes in multi-level and surface electrode traps is common and necessary (see Section 3.4.3,) the gaps are typically small compared to the electrode dimensions. The effects of the gaps on this analysis are further discussed in next section. From the integral given in (21), the potentials for bounded electrodes (rectangular) and infinite strips can be derived. The potentials given

in [61] are in terms of rectangular dimensions of the electrode. The same technique can be used to determine the potentials of non-rectangular bounded shapes numerically, which can give improved results over commonly used finite-element methods.

Based on the analysis of the electrode shapes discussed in [60, 61], another technique to design the electrode shapes and dimensions is proposed by and being used by the QIS group. This is the optimization technique referred to as "geometric compensation." Ion micromotion, as discussed in the previous section, is caused by DC fields pulling the ion out of the RF null and into the RF fields if the RF and DC nulls are not coincident. The procedure of producing a coincidence of the DC and RF nulls is called compensation. In geometric compensation optimization, the electrode sizes are determined that result in a pre-chosen voltages and a trapping center. The q parameter can be formulated using a linear electrode dimension as in (15). Using the corresponding conformal transformation to arcs, one can determine the optimized values of the arc angles and then determine the electrode dimensions for a given trap center and voltage set. Designing electrodes using this technique can significantly reduce the number of electrodes that have to be controlled to achieve compensation, simplifying the compensation process and reducing the interconnects required for scalable QIP.

3.5.1.5 Gaps

Segmentation of the control electrodes is necessary for axial ion motion control and stability. The previous discussion of analytical electrostatic model of rectangular and infinite-stripe electrodes has assumed gapless electrodes. In recent work [64], the electrostatics of electrodes with finite gaps were analyzed. The study suggested that it is safe to ignore the effects of gaps as long as the gap dimensions are small compared to the electrode-ion spacing. Even the non-realistic case of gaps equal to half of the ion height from the surface-electrode trap only result in the effect of gap to be $\sim 5\%$ for rectangular and infinite-strip electrodes. The case of finite gap aspect-ratio of 0.1, typically used in recent traps, the

effect is only $\sim 2\%$, which is negligible for standard modeling. However, from the fabrication standpoint the gaps between RF-DC electrodes and DC-DC electrodes need to be carefully optimized to avoid arcing and photo-lithographic errors as will be discussed in Section 3.5.3. Depending upon the choice of materials, gap dimensions smaller than $4\mu m$ between two conducting planes can be problematic in vacuum operations due to arcing. This issue is further discussed in Section 3.5.3.1.

For two- and three-level traps the gap considerations are more critical than the surface-electrode traps as discussed in [56] and in Section 3.4.1. The aspect ratio (α), efficiency parameter (η) and the ratio of gap to electrode thickness (δ) affect the secular frequencies and trapping depths. As shown in [56] the trapping depth for smaller values of α is larger. As α gets larger the depth gets smaller asymptotically. Similarly, for the two-level geometry, the efficiency η decreases with increased α requiring the ion distance from the electrode surfaces to be approximately ten times larger than the vertical electrode spacing.

In the design process it is common to use numerical simulation codes such as Finite Element Method (FEM), Finite Difference Method (FDM), Finite Integration Method (FIM), and Boundary Element Method (BEM). Several commercial packages are available to simulate the electrostatics of the trap geometry. Analytical methods discussed here, are usually cross-checked with numerical simulations.

3.5.2 Experiment-specific considerations

Although the microfabricated traps are designed to be used in a variety of QIP experiments, the geometries can be optimized for a particular experimental situation. Since more and more experiments require trapping multiple ions in 1D or 2D lattices, it is becoming a standard design requirement to be able to trap multiple ions. Additionally, experiments may require incorporating multiple zones such as loading zone, storage zone, computing zone, and junctions in the trap geometry. Trapping characteristics and the trap geometry are also optimized for the ion being trapped, optical access for loading, cooling, and gate laser beams, and collection efficiency.

3.5.2.1 Ion loading

The atoms used to form ions are typically produced by heated ovens emitting atoms into the trapping region where the ionizing and cooling beams overlap. In multi-level traps and surface-electrode traps the atom beam is introduced by adding through-substrate slots. In surface-electrode traps, even though the ions can be loaded on the front-side (active-side), it is safer to load ions by a through-substrate loading slot. This avoids the deposition of conductive layer from the oven that can span the electrode gaps and potentially short the electrodes. In multi-level traps, the oven is typically placed using vertical geometrical symmetry and shielding. If the ion trap is a multi-zone trap, the slot shape can be designed to minimize the pseudopotential deformation and maintain the ion position stably. Alternatively, the loading slot can span the entire trapping region. in this case the standard electrode optimization is used.

3.5.2.2 Optical access

The laser beam spot sizes at the ion location determine the loading slot dimensions. Laser waist beam sizes are typically in the 10 to 30 μm range. The slot widths should be of the order of at least five to ten times this dimension in order to avoid excess laser beam scattering from slot edges. This scattered light can obscure the ion fluorescence.

To cool the ions efficiently, the three principal axes of the trap pseudopotential must have nonzero components along the laser direction [65]. In particular, none of the principal axes can be vertical if the cooling beam is parallel to the horizontal trap surface for a planar trap. The necessary tilt in the principal axes relative to the beam direction is typically realized by using asymmetric electrode designs and/or setting the voltages in an asymmetrical manner. For multi-level traps, since the ion is trapped in the electrode plane, the beams are brought through the slot (RF electrodes separation) at an angle or orthogonally. With the slot openings of hundreds of microns, access in multi-level traps is usually less of a challenge. However, for the smaller dimensions in microfabricated traps, designing dimensions for optical access becomes a challenge. Avoiding light-scattering from the electrodes

is particularly important in design phase. In the case of a surface trap, the trap-chip has to be laid-out in such a way that laser beams propagating parallel to the surface of the chip can reach the ion without interruptions caused by wire-bonds and other features of the system.

3.5.2.3 Linear chains

Many experiments for QIP rely on ion chains. When the axial potential has conventional harmonic form, ion chains become unstable as the number of ion increases. The trapping potential and mutual Coulomb repulsion between ions start "squeezing" the ions trapped at the center of the chain. This squeezing can deform the shape of the 1D crystal to form zig-zags and other complicated shapes. According to one estimate [51] the anisotropy of the trap (ratio of radial and axial frequencies) has to be at least $\omega_{x,y}/\omega_z > 0.77N/\sqrt{\log N}$ to keep a stable linear-chain of the ions in a harmonic axial potential. If the ion-ion distance is kept equal throughout the length of the chain using an anharmonic axial potential, the chain will remain stable for infinite number of ions as long as the radial frequencies meet the condition $\omega_{x,y}^2 > 4.2e^2/(md^3)$ [65]. Here, e and m correspond to the charge and mass of an ion respectively, and d corresponds to the ion-ion distance. The axial potential can be shaped to provide the confinement of the ions in positions so that the ion-ion distance remains uniform along the chain. However, keeping the ion-ion spacing big enough for operating the entangling gates efficiently across the chain [51] and uniform with axial harmonic potential is difficult. One way to achieve uniform ion-ion spacing is to create an axial flat-bottomed potential or by adding anharmonicity into the axial harmonic potential. Anharmonic potentials relax the squeezing of the ions that are near the center of the chain. An alternative approach, being used by QIS group optimizes the electrode parameters not directly for the ion spacings, but for an objective function that measures the deviation of the resulting fields from a target analytic field that gives approximately uniform separation in the limit of a large number of ions. This approach will be discussed in detail in the context of a new trap design in Chapter 5.

Experimentally, in addition to having uniform ion-ion spacing through the chain length

for stability, the principal trapping axes of the ions need to be maintained at a constant value for radial-mode gates. In addition to requirements imposed by quantum gates, some quantum simulation experiments with linear chains also require individual addressing of ions in the chain. The ion-ion spacing required for such experiments should be uniform and of the order of gate-beam spot diameters ($\sim 10\ \mu m$).

3.5.2.4 Ions merging and splitting

The shuttling-based experiments for trapped-ions QIP rely on merging and splitting of ions in an array [52]. Ideally, merging and splitting is achieved while keeping the secular frequencies constant so that cooling can continue as efficiently as with the stored ions. Splitting an ion-chain into two halves or other ratios can be seen as an introduction of a potential barrier between two chain segments or a creation of a double-harmonic well. This barrier is produced by changing the potentials on a series of control electrodes without impacting the chain stability. In the design phase the simulation studies are useful to optimize the electrode dimensions and the number of electrodes for chain separation. A detailed study of the electrode configurations and geometries for fast splitting of ions from a string is given in [66]. By constraining the maximum voltage applied on each DC electrode and including all the electrodes to create the double-well, the electrode configurations can be found that achieve this using octupole electric fields. The octupole fields contain symmetry that avoids a linearly varying electric potential at the origin. Two-level, three-level, and surface-electrode geometries are compared for achieving large DC octupole moments in [66]. This study finds that three-level designs offer the largest octupole co-efficient for higher aspect ratios $\alpha \gg 1$, while two-level traps have better octupole with an aspect ratio of $\alpha \sim 0.5$. Surface-electrode traps of comparable size have ~ 150 times reduction in the octupole coefficient.

3.5.2.5 Transport of ions

For the experiments required in large-scale quantum computation proposals, junctions and multi-zone traps are designed. These geometries need to be designed to have multiple

modules within a trap-chip. During ion transport the axial potential is optimized to maintain a constant axial frequency to avoid parametric heating. During shuttling the potential to local minimum is kept harmonic. For efficient shuttling the electrodes are designed to have large potential overlap to achieve sufficiently fine control over the transport potential [63].

3.5.3 Fabrication considerations

Miniaturized ion trap designs have been built to date with printed circuit boards (PCB), conductive structure on substrate (CSS) and oxidized substrate, silicon on insulator (SOI), conductive structures on insulators, assembly of precision micro-machining, and lithographic technology on semiconductors [53]. Apart from selecting the geometry and electrode dimensions and shapes, the electrical characteristics of the trap may change based on the choice of materials. Since different fabrication processes deal with different materials, the electrical properties of the trap and choice of materials are inter-related considerations. Additionally, based on the fabrication technology being used and its capabilities, the geometries can have specific features, for example: buried wires can easily be incorporated into the geometry if the trap is being built using standard semiconductor technologies. In this section, electrical characteristics along with the choices of materials and other fabrication considerations are discussed.

3.5.3.1 Materials

The electrode material has to be highly conductive, resistive to severe oxidation, compatible with fabrication process, non-magnetic, and smooth. For ion traps, the DC electrodes and RF electrodes are typically made of same metal. In typical experiments, RF frequencies are in the range of 10 MHz – 100 MHz and the RF-peak voltages are in 50 V – 150 V. Since the experiments are conducted in ultra-high vacuum, in-vacuum RF arcing - also known as flashover or electrostatic discharge (ESD), is one of the major considerations in choosing the metal for RF electrode. RF arcing starts from electron emission from the interface between the metal and a dielectric in vacuum. Any imperfection or sharp corner feature

increases the local field and enhances the arcing. The material choice in combination with the inter-electrode gaps are to be considered in design phase. Depending upon the choice of the metal, in-vacuum arcing could limit the minimum gaps that can be used. In-air and in-vacuum tests on Al, brass, and Ni showed that the minimum gap that can used between electrodes for the typical RF voltages used is ~4 μm [67].

The electrode metal has to be non-magnetic since magnetization can decohere the quantum system. One of the models, explaining the anomalous ion-heating is the "patch-potential" model. In a recent study several electrode metal materials for ion traps were compared in relation to ion-heating [68]. Metals with smoother and inert surfaces are found to be preferable. Ion trap vacuum chambers are typically baked at temperature $\geq 200°C$. Due to this vacuum baking annealing effects on materials is another factor to be considered. At high temperatures, stress incompatibilities have shown nucleation of migrated grains to cause hammocks and extruded whiskers [69]. Careful attention should be paid to the interfacial properties of the layered materials. The electrical characteristics due to differences in work-functions can cause stray fields that can impact the electrical behavior of the trap.

The choice of dielectric material for insulation is mainly dictated by the voltage breakdown and loss for the applied RF. The breakdown voltage depends upon the dielectric strength, E_c. Dielectric strength depends upon the thickness. Based on the studies in [70], $E_c \propto d^{-\alpha}$, where $\alpha = 1.01$ for thicknesses 25-250 Å and $\alpha = 0.59$ for thicknesses 250-2500 Å. Another important factor is the RF loss tangent. Using the complex permittivity of the dielectric, $\epsilon = \epsilon^{'} + \epsilon^{''}$, the loss tangent is $\tan\delta \approx \epsilon^{''}/\epsilon^{'}$. The dielectric loss tangent is related to the power dissipation by [53]

$$P_d = \frac{V_{ac}^2 \Omega_{RF}^2 C^2 R (1 + \tan^2\delta)^2}{2(1 + \Omega_{RF}^2 C^2 R^2 (1 + \tan^2\delta)^2)}\,, \tag{22}$$

where V_{ac} is applied RF voltage, Ω_{RF} is RF frequency, C and R are electrode capacitance and resistance. The loss tangent needs to be small enough to avoid heating and low Q resonant circuits. Loss tangents of $10^{-}3$ are typically required. Minimizing electrode capacitance is another factor in choosing the dielectric material.

The choice of substrate depends upon the fabrication technology used and the geometry of the trap. Traps with the substrates ranging from highly-doped semiconductors to low-loss dielectric have been demonstrated [53]. Considering geometry, dimensions, and fabrication technology, the choice of the substrate is made during the design phase.

3.5.3.2 Technology considerations

The fabrication method chosen for ion traps should be robust enough to generate repeatable process results. Due to the requirements of repeatability and low-dimensionality, semiconductor technologies have been demonstrated to be superior that the other fabrication technologies. For traps with dimensions in the range of hundreds of microns, several other techniques can be used [53], and in most cases these traps are built with either micromachining or bonded substrates. The non-monolithic fabrication processes lack the level of uniformity, repeatability, and accuracy obtained with that the semiconductor-based processes. It has been challenging to scale-up the processes by producing a larger number of trap locations. Semiconductor fabrication excels at achieving this scaling requirement.

For the experiments using ions arrays, the traps are more useful and versatile if they have smaller dimensions and a larger number of control electrodes. Smaller electrodes ($< 100/micron$) provide better control over the voltages to generate potentials that can trap uniform chains, merge and split chains, transport ions, and manipulate radial fields to compensate. Researchers are at present utilizing more traps that are built with semiconductor technologies [71, 53, 56, 72]. Although there are many factors which dictate the primary design of the trap, fabrication capabilities and process robustness are critical in successful trap demonstrations. Design-for-fabrication is a common process component in micro-electromechanical (MEMS) structures.

CHAPTER 4

STABILITY ANALYSIS OF MOTION OF AN ION IN ASYMMETRIC PLANAR TRAPS

In the quest to miniaturize ion traps for QIP, many of the recent designs being explored are planar versions of linear Paul traps [59, 73, 74]. Since the electrodes all lie in a single plane, these traps can be constructed using VLSI microfabrication, which offers greater scalability and potential to be integrated with other useful on-chip components such as mirrors, fiber ferrules, cavities, and junctions [53]. The ions trapped by a surface-electrode trap are cooled by laser beams that are commonly aligned parallel to the trap surface. In order to cool a single ion efficiently, the three principal axes of the trap pseudopotential must have nonzero components along the laser direction [65]. In particular, none of the principal axes can be vertical, if the cooling beam is parallel to the horizontal trap surface. The necessary tilt in the principal axes relative to the beam direction is typically realized by using asymmetric electrode designs and/or by setting the voltages in an asymmetrical manner. In general, such an asymmetry introduces a relative angle between the principal axes of the RF and DC fields [72] (See Figure 12). When the angle between the RF and DC principal axes is nonzero, the classical equations of motion of a single ion near the trap center are given by a coupled version of the Mathieu equation. The stability properties of such a coupled system cannot be obtained from the classical stability analysis of Paul traps, which assumes that the equations are decoupled. Thus, it is not clear, a priori, that the trap operating conditions obtained from the stability analysis of symmetric Paul traps will result in stable ion motion in asymmetric surface traps, as well. One needs to do the stability analysis for the asymmetric case from scratch, and obtain the corresponding stable operating conditions.

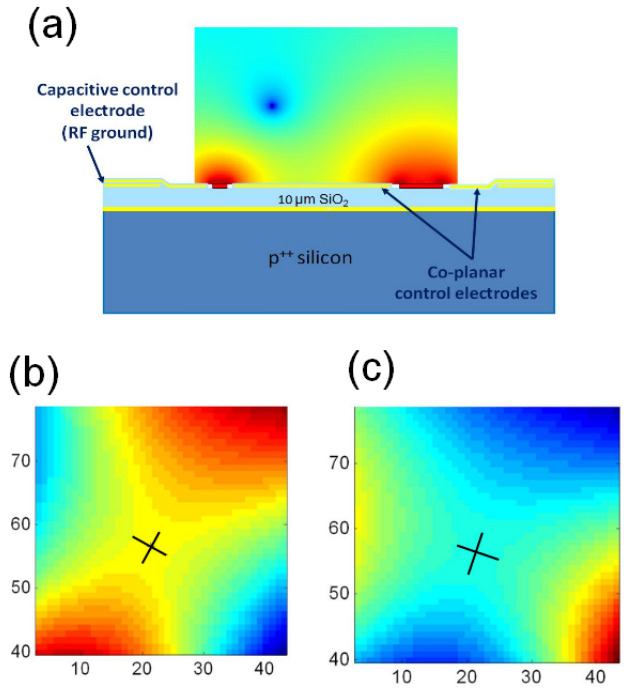

Figure 12: The cross-section of first-generation of the surface trap built by QIS [75] and the associated potentials shown as an example. In (a), the trap axis and the long RF electrodes (shown in red) are orthogonal to the page. The DC control electrodes above the substrate are shown in yellow. The total pseudopotential is shown as a color density plot, with the minimum of the pseudopotential, i.e., the trap center, being shown in in blue. In Figures (b) and (c), we show the RF and DC potentials near the trap center, respectively. These potentials were calculated numerically using the trap geometry and voltages. The RF and DC principal axes are not aligned perfectly, and have a small angle between them. Due to this nonzero relative angle, the ion motion in the radial directions is coupled.

This chapter discusses my research published in [76]. In this work, the stability diagrams for asymmetric surface traps, or more generally, for trap designs and operating conditions that result in a relative angle between the radial principal axes of RF and DC fields, are obtained. The diagrams generalize the standard q-a stability diagrams for symmetric Paul traps, and provide stable operating conditions for traps for which the RF and DC principal axes are not aligned. While the analysis is for the motion of a single ion, the results are also applicable to the center-of-mass motion of a collection of ions with equal masses, in a harmonic trap. In the reference [76] numerical and analytical studies are shown; here, only the analytical approach is presented. This approach utilizes the *multi-scale perturbation theory*, also known as the *method of multiple scales* [77, 78], to obtain

approximations to the curves bounding the primary stability region. These approximate results take the form of formulas that relate the parameters describing the system, such as q, a and the angle between the RF and DC principal axes.

4.1 Equations of motion

Let us begin by writing the general equations of motion of an ion near the center of an asymmetrical trap. We will assume that the oscillating (RF) and static (DC) electric fields have a coincident zero at the trap center, which we take to be the origin of our coordinate system. We will work in the harmonic approximation, treating the potentials as second order in the displacements from the origin, and forces (or electric fields) as first order. Since the electric fields vanish at the origin, the potential has no first order terms. Denoting the potential energy of an ion by $U = eV$, where e is the ion charge, and choosing the zero of U so that $U(\mathbf{0}) = 0$, we have, up to second order in the displacements,

$$\begin{aligned} U(\mathbf{x}, t) &= U^{\mathrm{RF}}(\mathbf{x}) \cos \Omega_{\mathrm{RF}} t + U^{\mathrm{DC}}(\mathbf{x}) && (23) \\ &= \frac{1}{2} \sum_{ij} x_i x_j \left(U_{ij}^{\mathrm{RF}} \cos(\Omega_{\mathrm{RF}} t) + U_{ij}^{\mathrm{DC}} \right) , && (24) \end{aligned}$$

where x_i with $i = 1, 2, 3$ stand for x, y, z, respectively, Ω_{RF} is the RF angular frequency, and the U_{ij}^{RF} and U_{ij}^{DC} are the matrices of second derivatives of the RF and DC potential energies.

The equations of motion are given as,

$$\begin{aligned} m \frac{d^2 x_i}{dt^2} &= -\frac{\partial U}{\partial x_i} && (25) \\ &= -\sum_j x_j \left(U_{ij}^{\mathrm{RF}} \cos(\Omega_{\mathrm{RF}} t) + U_{ij}^{\mathrm{DC}} \right) . && (26) \end{aligned}$$

Defining a new time variable τ by $\Omega_{\mathrm{RF}} t = 2\tau$ and denoting the derivatives with respect to τ by dots, we get,

$$\ddot{x}_i + \sum_j A_{ij} x_j + 2 \sum_j Q_{ij} x_j \cos 2\tau = 0 , \qquad (27)$$

where,

$$A_{ij} = 4U_{ij}^{\mathrm{DC}} / m\Omega_{\mathrm{RF}}^2 , \qquad Q_{ij} = 2U_{ij}^{\mathrm{RF}} / m\Omega_{\mathrm{RF}}^2 , \qquad (28)$$

are the multi-variable versions of the stability parameters a and q of the Mathieu equation [61]. Like U^{DC} and U^{RF}, the matrices $\mathbf{A}$ and $\mathbf{Q}$ are both traceless. In the case of diagonal $\mathbf{A}$ and $\mathbf{Q}$, the equations (27) reduce to three decoupled copies of the Mathieu equation. Using the stability diagram of the Mathieu equation, one obtains the standard q-a stability diagrams of symmetric Paul traps [47, 46].

In most surface trap designs, the RF electrodes are long, and the total RF field has non-vanishing components only in the radial directions, which we denote by x and y. If, in addition, the electrode shapes and voltages are symmetric around the $z = 0$ plane, which is commonly the case, the motion along the z-direction (the axial motion) decouples from the radial motion. Note that in order for the axial motion to be confined, A_{zz} must be positive.

Under this symmetry assumption, the x-y equations of motion are also of the form (27), but the matrices $\mathbf{A}$ and $\mathbf{Q}$ are now 2×2. Since the original, 3×3 matrix $\mathbf{A}$ was traceless and $A_{zz} > 0$, the 2×2 version of this matrix must have negative trace. This means that the DC field must be anti-confining in at least one of the radial directions. Since the z-component of the RF field is assumed to be zero identically, the 2×2 version of the matrix $\mathbf{Q}$ is traceless.

In order to investigate the stability properties of the 2×2 version of the system (27), we next pick a convenient coordinate system. Since the matrices $\mathbf{Q}$ and $\mathbf{A}$ are both symmetric, they can separately be diagonalized by suitable rotations. We will assume that $\mathbf{A}$ is diagonalized, and write it in the form, $\mathbf{A} = a\left(\begin{smallmatrix} 1 & 0 \\ 0 & -\alpha \end{smallmatrix}\right)$, where where a and α are constants to be determined by the electrode geometry and the DC voltages. As mentioned above, $\mathbf{A}$ must have negative trace due to Gauss's law and the fact that the ion is confined along the z-axis. Thus, we must either have $a > 0$ and $\alpha > 1$, or $a < 0$ and $\alpha < 1$ in order to have the ion confined along the z direction. In our calculations below, we will focus on the case $\alpha > 0$. In order to have confinement along the z-axis, $\alpha < 0$ would need to be accompanied with $a < 0$, and this pair of conditions would correspond to the DC potential being anti-confining in both of the radial axes. Although this is possible, such potentials are not frequently encountered in surface trap designs used in practice.

Let us next turn to $\mathbf{Q}$. Recall that U_{ij}^{RF} is symmetric and traceless. If we were to use a coordinate system $(\tilde{x}, \tilde{y})$ in which U_{ij}^{RF} is diagonal, the amplitude of the RF potential energy would have the form,

$$U^{\mathrm{RF}}(\tilde{x}, \tilde{y}) = \frac{1}{2} U_0^{\mathrm{RF}}(\tilde{x}^2 - \tilde{y}^2)\,, \tag{29}$$

and Q_{ij}, would be given through (28) as, $\mathbf{Q} = q\left(\begin{smallmatrix} 1 & 0 \\ 0 & -1 \end{smallmatrix}\right)$ where q is a free parameter. The two coordinate systems, $(\tilde{x}, \tilde{y})$ (in which $\mathbf{Q}$ is diagonal) and (x, y) (in which $\mathbf{A}$ is diagonal) are related by a rotation,

$$\tilde{x} = x\cos\theta + y\sin\theta \tag{30}$$

$$\tilde{y} = -x\sin\theta + y\cos\theta\,, \tag{31}$$

where θ is the angle of rotation. Substituting these in (29), we get the RF potential energy in terms of the coordinates along the DC principal axes. Using (28), we get the resulting $\mathbf{Q}$ matrix as, $\mathbf{Q} = q\left(\begin{smallmatrix} \cos 2\theta & \sin 2\theta \\ \sin 2\theta & -\cos 2\theta \end{smallmatrix}\right)$. Finally, using $\mathbf{A}$ and $\mathbf{Q}$, the radial version of the equations of motion (27) become,

$$\ddot{x} + ax + 2q(cx + sy)\cos 2\tau = 0 \tag{32}$$

$$\ddot{y} - \alpha a y + 2q(sx - cy)\cos 2\tau = 0\,, \tag{33}$$

where for brevity we replaced $\cos 2\theta$ and $\sin 2\theta$ by c and s, respectively. The classic case of symmetric Paul traps where $\theta = 0$ is recovered by setting $s = 0$ and $c = 1$.

4.2 Approximation with the method of multiple scales

For a given set of parameters, it would be beneficial to have approximate analytical formulae for the stability boundaries. Such approximate formulae would enable trap designers to quickly check the stability regions for a particular trap geometry, and would guide the trap design. Analogous results for the case of symmetric traps are well-known and useful.

One possible approach to this problem is to use straightforward perturbation theory of ordinary differential equations, which involves treating a certain parameter (q, in our

case) as small, and expanding the unknown function into a power series in terms of this parameter. This gives separate equations for each power of the perturbation parameter, which are then solved order by order. While useful in many settings, this approach fails for a variety of problems -including the Mathieu equation- due to the appearance of so-called "secular", or "resonant" terms, which grow in time in an unbounded manner even when the exact solution is known to be bounded. This behavior invalidates the assumptions in the perturbation analysis after a certain time period.

Multi-scale perturbation theory, or the method of multiple scales, is a more sophisticated technique, capable of avoiding secular terms by expanding not only the solution, but also the independent parameter (typically, time) to a series in the small parameter. This results in a set of *partial* differential equations (PDEs) that collectively represent the ordinary differential equation under consideration. The solutions of these PDEs are then restricted by imposing the condition that secular terms do not appear. In this way, the method of multiple scales can give uniformly accurate results for cases where standard perturbation theory gives results valid only for short time intervals. In this section, we will use this technique to obtain approximate stability boundaries for the coupled system, (32)-(33). There are various conventions followed in the literature on the method of multiple scales. Below, we will use the approach described in [78] and [77]. For an elementary introduction to the method of multiple scales, see [79, 78]. For applications to the coupled Mathieu system, see [77, 80].

We would like to obtain approximate formulas for $a(q)$ on the stability boundaries of the the coupled Mathieu system (32)-(33), which we reproduce here:

$$\ddot{x} + ax + 2q(cx + sy)\cos 2\tau = 0 \tag{34}$$

$$\ddot{y} - \alpha ay + 2q(sx - cy)\cos 2\tau = 0\,. \tag{35}$$

These equations describe the radial motion of an ion in an asymmetric trap with decoupled axial motion. The system (34)-(35) has multiple regions of stability separated by regions

of instability (or regions of partial stability); we will focus on the primary stability region near the origin of the a-q plane and its immediate surroundings. We will treat q as a small variable, and perform an expansion in its powers.

The main idea of multi-scale perturbation theory is to introduce a set of slowly-varying time variables (the "multiple scales"), $T_0 = \tau$, $T_1 = q\tau$, $T_2 = q^2\tau, \ldots$. We replace the dependent variables x and y with functions of the T_is,

$$x(\tau) = x(T_0, T_1, \ldots) \tag{36}$$

$$y(\tau) = y(T_0, T_1, \ldots) \tag{37}$$

and expand the latter into series in q,

$$x = x_0(T_0, T_1) + qx_1(T_0, T_1) + q^2x_2(T_0, T_1) + \ldots \tag{38}$$

$$y = y_0(T_0, T_1) + qy_1(T_0, T_1) + q^2y_2(T_0, T_1) + \ldots . \tag{39}$$

The chain rule gives the derivative with respect to τ in terms of partial derivatives with respect to the time variables T_i,

$$\frac{d}{d\tau} = \frac{\partial}{\partial T_0} + q\frac{\partial}{\partial T_1} + q^2\frac{\partial}{\partial T_2} + \ldots \tag{40}$$

Substituting (36), (37), (38), (39) and (40) into (34)-(35) and obtaining separate equations for each power of q, one gets the equations for multi-scale perturbation theory. For generic values of a, these equations can be solved to get approximate solutions to (34)-(35) that are valid for small values of q. However, if a is close to certain critical values, this procedure breaks down due to the appearance of so-called *small denominators*. These critical values are of special interest to us, since they are the locations where the stability boundaries intersect the $q = 0$ axis [78]. Various approaches exist for dealing with these critical points; we will follow the technique used in [78], which consists of expanding a into a series in powers of q around these points. If a_0 is such a critical value, we set

$$a = a_0 + a_1q + a_2q^2 + \ldots . \tag{41}$$

It is noted in [77] that in order to get results accurate to order q^2, it suffices to work with T_0 and T_1, which is what we will do in the following section.

4.2.1 Multi-scale expansion of the two-variable Mathieu system

We begin by obtaining the general multi-scale expansion for the equations of motion (34)-(35). Evaluating $\frac{dx}{d\tau}$, $\frac{dy}{d\tau}$, $\frac{d^2x}{d\tau^2}$ and $\frac{d^2y}{d\tau^2}$ using (38), (39), (40), substituting the expansion (41), and collecting terms with similar powers of q up to the second order, we get,

$$D_0^2 x_0 + a_0 x_0 = 0 \tag{42}$$

$$D_0^2 x_1 + a_0 x_1 = -2D_0 D_1 x_0 - a_1 x_0 - 2(cx_0 + sy_0)\cos 2T_0 \tag{43}$$

$$D_0^2 x_2 + a_0 x_2 = -2D_0 D_1 x_1 - D_1^2 x_0 - a_1 x_1 - a_2 x_0 - 2(cx_1 + sy_1)\cos 2T_0 \tag{44}$$

for (34), and,

$$D_0^2 y_0 - \alpha a_0 y_0 = 0 \tag{45}$$

$$D_0^2 y_1 - \alpha a_0 y_1 = -2D_0 D_1 y_0 + \alpha a_1 y_0 - 2(sx_0 - cy_0)\cos 2T_0 \tag{46}$$

$$D_0^2 y_2 - \alpha a_0 y_2 = -2D_0 D_1 y_1 - D_1^2 y_0 + \alpha a_1 y_1 + \alpha a_2 y_0 - 2(sx_1 - cy_1)\cos 2T_0 \tag{47}$$

for (35), where D_i denotes $\frac{\partial}{\partial T_i}$.

Following our discussion in Section 4.1, we will assume $\alpha > 0$. For the primary stability region near the origin for $a \geq 0$, the relevant critical values that determine the stability boundaries are $a_0 = 0$ and $a_0 = 1$ (See [77] for the details of the relevant calculation for a coupled Mathieu system). In Section 4.2.1.3, we will obtain the results for $a < 0$ from those for $a > 0$ by a simple transformation. The expansion around $a = 0$ will proceed similarly to the single variable case as discussed in [78, 77], but the case $a = 1$ requires special attention.

Motivated by the empirical empirical observation of numerical results in [76], we will obtain formulas for the curves emanating at the critical point $a_0 = 1$, and use them as stability boundaries after they intersect with the curves emanating from $a_0 = 0$. We will demonstrate the reliability of this approach in the stability plots we present below.

4.2.1.1 *Expansion around $a = 0$*

We begin with the expansion around $a = 0$. Setting $a_0 = 0$ in equations (42)-(47), we get,

$$D_0^2 x_0 = 0 \tag{48}$$

$$D_0^2 x_1 = -2D_0 D_1 x_0 - a_1 x_0 - 2cx_0 \cos 2T_0 - 2sy_0 \cos 2T_0 \tag{49}$$

$$D_0^2 x_2 = -2D_0 D_1 x_1 - D_1^2 x_0 - a_1 x_1 - a_2 x_0 - 2cx_1 \cos 2T_0 - 2sy_1 \cos 2T_0\,, \tag{50}$$

and,

$$D_0^2 y_0 = 0 \tag{51}$$

$$D_0^2 y_1 = -2D_0 D_1 y_0 + \alpha a_1 y_0 + 2cy_0 \cos 2T_0 - 2sx_0 \cos 2T_0 \tag{52}$$

$$D_0^2 y_2 = -2D_0 D_1 y_1 - D_1^2 y_0 + \alpha a_1 y_1 + \alpha a_2 y_0 + 2cy_1 \cos 2T_0 - 2sx_1 \cos 2T_0\,. \tag{53}$$

Solving (48) and (51) and setting the secular terms to zero, we get,

$$x_0(T_0, T_1) = A(T_1) \tag{54}$$

$$y_0(T_0, T_1) = C(T_1)\,. \tag{55}$$

Substituting these in (49) and (52) gives,

$$D_0^2 x_1 = -a_1 A(T_1) - 2(cA(T_1) + sC(T_1)) \cos 2T_0 \tag{56}$$

$$D_0^2 y_1 = \alpha a_1 C(T_1) + 2(cC(T_1) - sA(T_1)) \cos 2T_0\,. \tag{57}$$

In order to avoid growing terms in x_1 and y_1, we need to pick $a_1 = 0$. Solving (56) and (57) with this assumption and setting the coefficients of two other secular terms that grow linearly in T_0 to zero, we get,

$$x_1(T_0, T_1) = B(T_1) + \frac{1}{2}(cA(T_1) + sC(T_1)) \cos 2T_0 \tag{58}$$

$$y_1(T_0, T_1) = D(T_1) + \frac{1}{2}(sA(T_1) - cC(T_1)) \cos 2T_0\,. \tag{59}$$

Plugging the solutions (54), (55), (58), (59) in (50) and (53), we get equations for x_2 and y_2. These will have bounded solutions only if the T_0-independent terms on the right hand

sides add up to zero. Asserting this condition gives,

$$A''(T_1) + \left(a_2 + \frac{1}{2}(c^2 + s^2)\right)A(T_1) = 0 \tag{60}$$

$$C''(T_1) + \left(-\alpha a_2 + \frac{1}{2}(c^2 + s^2)\right)C(T_1) = 0\,. \tag{61}$$

Equations (60) and (61) will have oscillatory solutions for $A(T_1)$ and $B(T_1)$ when $a_2 > -\frac{1}{2}(c^2 + s^2)$, and when $a_2 < \frac{1}{2\alpha}(c^2 + s^2)$, respectively. With $s^2 + c^2 = 1$ and assuming $\alpha > 0$, we see that simulatenous stability occurs for $-\frac{1}{2} < a_2 < \frac{1}{2\alpha}$. In other words, the stability boundaries around $a = 0$ are given by,

$$a = -\frac{1}{2}q^2 \tag{62}$$

$$a = \frac{1}{2\alpha}q^2\,. \tag{63}$$

Note that these conditions are what would be obtained from separate stability analyses of (34) and (35), respectively, if the coupling terms in those equations were ignored.

4.2.1.2 Expansion around $a = 1$

We next expand around $a = 1$. As mentioned above, in this case we will seek solutions with partial stability. For $a_0 = 1$, (42)-(44) become,

$$D_0^2 x_0 + x_0 = 0 \tag{64}$$

$$D_0^2 x_1 + x_1 = -2D_0D_1x_0 - a_1x_0 - 2(cx_0 + sy_0)\cos 2T_0 \tag{65}$$

$$D_0^2 x_2 + x_2 = -2D_0D_1x_1 - D_1^2x_0 - a_1x_1 - a_2x_0 - 2(cx_1 + sy_1)\cos 2T_0\,, \tag{66}$$

and (45)-(47) become,

$$D_0^2 y_0 - \alpha y_0 = 0 \tag{67}$$

$$D_0^2 y_1 - \alpha y_1 = -2D_0D_1y_0 + \alpha a_1y_0 - 2(sx_0 - cy_0)\cos 2T_0 \tag{68}$$

$$D_0^2 y_2 - \alpha y_2 = -2D_0D_1y_1 - D_1^2y_0 + \alpha a_2y_0 + \alpha a_1y_1 - 2(sx_1 - cy_1)\cos 2T_0\,. \tag{69}$$

The general solution to (64) is,

$$x_0(T_0, T_1) = A(T_1)\cos T_0 + B(T_1)\sin T_0\,. \tag{70}$$

Assuming $\alpha > 0$, the solution to (67) is exponential,

$$y_0(T_0, T_1) = E(T_1) \exp(\sqrt{\alpha} T_0) + F(T_1) \exp(-\sqrt{\alpha} T_0) . \tag{71}$$

This shows that the general multi-scale solution to the coupled system is at least partially unstable for $\alpha > 0$, $a_0 = 1$, as we observed in our discussed above. In order to investigate partial stability, we set the coefficients of the exponential solutions to zero, $E(T_1) = 0 = F(T_1)$, which gives $y_0(T_0, T_1) = 0$. Substituting $y_0 = 0$ and the solution (70) in (65), and setting the coefficients of $\sin T_0$ and $\cos T_0$ on the right hand side to zero in order to avoid resonant (secular) terms that would result in growing solutions for x_1, we get,

$$2A' - (a_1 - c)B = 0 \tag{72}$$

$$2B' - (a_1 + c)A = 0 . \tag{73}$$

Combining these, we get,

$$A'' = -\frac{a_1^2 - c^2}{4} A \tag{74}$$

$$B'' = -\frac{a_1^2 - c^2}{4} B , \tag{75}$$

which will have oscillatory solutions if $a_1^2 > c^2$ and exponential ones if $a_1^2 < c^2$. Thus, the critical values for partial stability are,

$$a_1 = \pm c . \tag{76}$$

The oscillating solutions for A and B are given as,

$$A(T_1) = r \sin \lambda T_1 + p \cos \lambda T_1 \tag{77}$$

$$B(T_1) = \frac{2\lambda}{a_1 - c}(-p \sin \lambda T_1 + r \cos \lambda T_1) , \tag{78}$$

where $\lambda = \sqrt{\frac{a_1^2 - c^2}{4}}$, and r and p are constants. After having ensured that the resonant terms in (65) vanish by enforcing (72) and (73), we can solve (65) to get the oscillatory solutions for x_1. We get,

$$x_1(T_0, T_1) = C(T_1) \cos T_0 + D(T_1) \sin T_0 + \frac{c}{8} A(T_1) \cos 3T_0 + \frac{c}{8} B(T_1) \sin 3T_0 . \tag{79}$$

Similarly, substituting $y_0 = 0$ and the solution (70) in (68), we get a bounded solution for y_1 after setting the coefficients of the exponential terms to zero:

$$y_1(T_0, T_1) = \frac{s}{(\alpha+1)}(A(T_1)\cos T_0 - B(T_1)\sin T_0) + \frac{s}{(\alpha+9)}(A(T_1)\cos 3T_0 + B(T_1)\sin 3T_0)\,. \tag{80}$$

We next substitute the solutions (79) and (80) into (66) and collect the resonance terms, i.e., terms proportional to $\sin T_0$ and $\cos T_0$, on the right hand side. Setting the coefficients of these resonances to zero in order to avoid growing solutions for x_2, we get,

$$2C'(T_1) + D(T_1)(-a_1 + c) = B(T_1)'' + \beta B(T_1) \tag{81}$$

$$2D'(T_1) + C(T_1)(a_1 + c) = -A''(T_1) - \beta A(T_1)\,, \tag{82}$$

where,

$$\beta = a_2 + \frac{c^2}{8} + \frac{2s^2(5+\alpha)}{(9+\alpha)(1+\alpha)}\,. \tag{83}$$

Using (74)-(75), we get,

$$2C'(T_1) + D(T_1)\,(-a_1 + c) = \mu B \tag{84}$$

$$2D'(T_1) + C(T_1)\,(a_1 + c) = -\mu A\,, \tag{85}$$

where $\mu = \beta - \lambda^2 = a_2 + \frac{c^2}{8} + \frac{2s^2(5+\alpha)}{(9+\alpha)(1+\alpha)} - \frac{a_1^2 - c^2}{4}$. Combining (84) and (85) with (72) and (73), we get the decoupled equations,

$$C'' + \frac{a_1^2 - c^2}{4}C = -\frac{\mu a_1}{2}A \tag{86}$$

$$D'' + \frac{a_1^2 - c^2}{4}D = -\frac{\mu a_1}{2}B\,. \tag{87}$$

Now, since the solutions (77) and (78) for A and B are in resonance with the left hand sides of (86) and (87), in order to avoid growing solutions, the coefficients on the right hand sides of these equations must vanish. Using (76), this gives,

$$a_2 = -\frac{c^2}{8} - \frac{2s^2(5+\alpha)}{(1+\alpha)(9+\alpha)}\,. \tag{88}$$

Thus, the second order approximation to the relevant stability boundary starting at $a = 1$ is given as,

$$a = 1 - cq - \left(\frac{c^2}{8} + \frac{2s^2(5+\alpha)}{(1+\alpha)(9+\alpha)}\right)q^2\,, \tag{89}$$

where we picked the negative sign for the first order term in order to get the curve that approximates the upper boundary of the primary stability region.

4.2.1.3 Boundary of the primary stability region.

In order to obtain the approximate boundaries of the primary stability region, we also need to find an approximate formula for the stability boundary that emanates from a negative cricital point of a when $q = 0$. Our expansion around $a = 1$ used the fact that to zeroth order, x has oscillatory solutions, and y has exponential ones when $a > 0$ (see equations (42) and (45)). In order to obtain the curves for negative a, we just use a series of redefinitions to replace the roles of x and y by. Namely, we set,

$$\tilde{x} = y\,,\ \tilde{y} = x\,,\ \tilde{a} = -\alpha a\,,\ \tilde{\alpha} = 1/\alpha\,,\ \tilde{c} = -c\,,\ \tilde{s} = s\,. \tag{90}$$

These redefinitions transform the equations of motion (34) and (35) into exactly the same form, with the variables (except q and τ) being replaced by their tilded counterparts,

$$\ddot{\tilde{x}} + \tilde{a}\tilde{x} + 2q(\tilde{c}\tilde{x} + \tilde{s}\tilde{y})\cos 2\tau \;=\; 0 \tag{91}$$

$$\ddot{\tilde{y}} - \tilde{\alpha}\tilde{a}\tilde{y} + 2q(\tilde{s}\tilde{x} - \tilde{c}\tilde{y})\cos 2\tau \;=\; 0\,. \tag{92}$$

Now, if $a < 0$, the transformation (90) makes $\tilde{a} > 0$, thus, since $\tilde{\alpha} > 0$ when $\alpha > 0$, we can use the approximate stability boundary (89) for (91)-(92) after replacing all the quantities in (89) by their tilded counterparts. This gives,

$$\tilde{a} = 1 - \tilde{c}q - \left(\frac{\tilde{c}^2}{8} + \frac{2\tilde{s}^2(5+\tilde{\alpha})}{(1+\tilde{\alpha})(9+\tilde{\alpha})}\right)q^2\,, \tag{93}$$

or, equivalently,

$$a = -\frac{1}{\alpha}\Big(1 - cq - \left(\frac{c^2}{8} + \frac{2s^2(5+1/\alpha)}{(1+1/\alpha)(9+1/\alpha)}\right)q^2\Big)\,. \tag{94}$$

This gives the missing approximate boundary of the primary stability region. Note that the curve starts at $a = -1/\alpha$. To summarize, the four approximate boundaries of the primary stability region are, (62), (63), (89) and (94).

In Figure. 13 to Figure. 19, we compare the results of this section with the results from the numerical analysis for various values of α and θ [76]. We note that the stability behavior of the system is symmetric around $\theta = 45°$, in the sense that the plots for $45° + \Delta\theta$ and $45° - \Delta\theta$ are identical (see Figure. 13). This is due to the fact that the equations of motion are invariant under the transformation $\theta \to \pi/2 - \theta$, $y \to -y$. Since the system is symmetric under reflections of the y axis, this transformation should leave the stability plot invariant. In Figure. 14 to Figure. 19, we only show the stability plots for θ between $0°$ and $45°$.

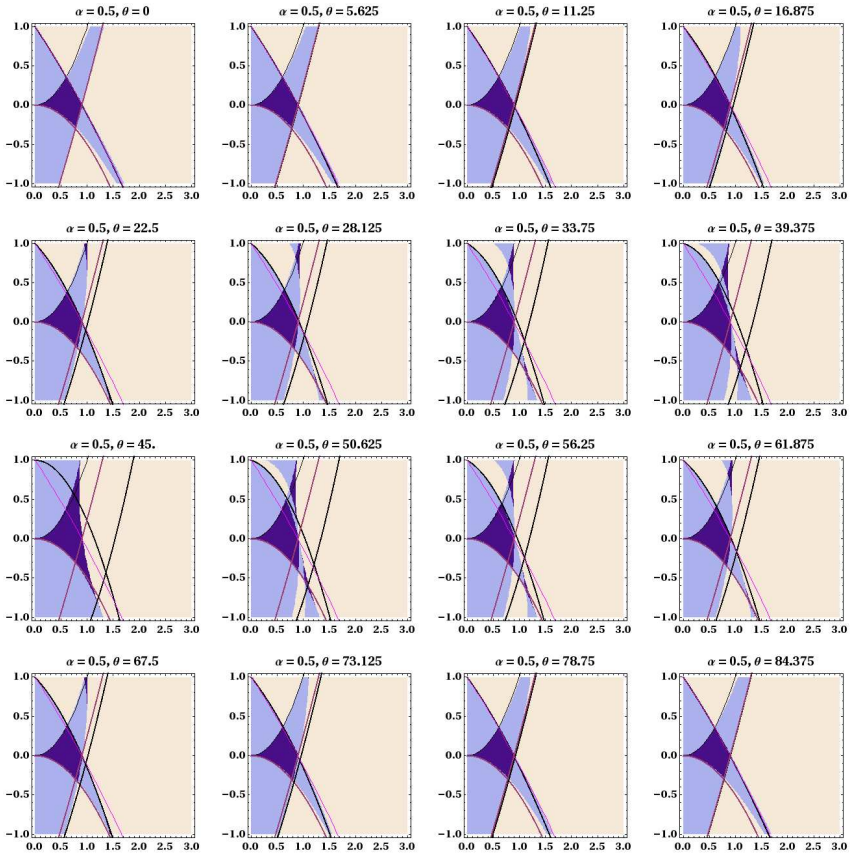

Figure 13: Stability plots for $\alpha = 0.5$ and θ between 0° and 90°, with a step size of 5.625°. The x-axis is q and the y-axis is a in each plot. The areas shown in dark purple correspond to complete stability, and those in blue correspond to partial stability, predicted using the numerical method. The black curves are the approximate stability boundaries for the coupled, two variable Mathieu system, obtained from equations (62), (63), (89), and (94). The magenta curves are the approximate stability boundaries for the corresponding *decoupled* system. We comment on the relation between the stability boundaries of the coupled and the decoupled systems in Section 4.3. Note that the approximate boundaries around $(q, a) = (0, 0)$ are identical for the coupled and the decoupled systems. (See equations (62), (63). We see that the black curves (for the coupled system) follow the partial stability boundaries quite accurately when q is small, however, when θ gets close to 45°, the curves starting at $(q, a) = (0, 1)$ and $(q, a) = (0, -1/\alpha) = (0, -2)$ lose their accuracy near the primary region of full stability. The colored curves representing the approximate boundaries of the *decoupled system*, while inaccurate predictors for the coupled system, consistently underestimate the size of the primary stability region. This behavior is observed in Figures 14 to 19, as well.

4.3 Conclusions and discussion

In Figures 13-19, we present the results of our stability analysis. We compare the stability regions predicted by the numerical method [76] (the purple regions,) to the stability boundaries obtained by the multi scale perturbation analysis (black lines). We show plots

for a range of angles θ between the RF and DC axes, and a range of αs (recall equations (32)-(33)). A few important conclusions are evident from the plots.

- The primary stability region *does not get smaller* when a nonzero angle θ is introduced between the RF and DC axes if the other variables are kept fixed. Such a nonzero angle between RF and DC fields represents the case of an asymetric surface electrode geometry and/or asymmetric voltages.

- Although the primary stability region does not change appreciably when θ is varied, two secondary stability regions are highly variable, and when θ has the special value of 45°, they join the primary region to result in an exceptionally large region of stability.

- The curves obtained from multi-scale perturbation theory approximate the boundaries of partial stability quite accurately when q is near zero. Regions of partial stability become regions of full stability when they "overlap" near the the location of the primary stability region of classical, symmetric Paul traps. Unfortunately, in this region, q seems to be large enough to make the accuracy of the approximation unsatisfactory, especially for angles θ close to the critical value of 45°. Since in practice, partial stability means instability, the small q region where our multi-scale formulas are uniformly accurate is not of relevance to the practical problem of the stability of ion motion.

- When we lay the approximate stability boundaries for the *symmetric* Paul trap (described by *decoupled* equations) on top of the coupled stability plots, we see that these boundaries consistently *underestimate* the size of the stability region for the coupled system.

The conclusion of our analysis for the practical problem of asymmetric ion trap design and operation is as follows: Just as in the case of symmetric Paul traps, the *q-a* stability

plot of the standard *single*-variable Mathieu equation is sufficient to allow one to determine stable operating conditions for asymmetric surface traps with long RF electrodes. It is possible to proceed as in the case of symmetric Paul traps, by obtaining a pair of "a" values for the two radial principal axes of the DC potential, and a pair of "q" values for the two radial principal axes of the RF potential. Ignoring the fact that there is a nonzero relative angle between the RF and DC axes, the two decoupled Mathieu equations for these (q, a) pairs can be used to determine the stability properties of the coupled system. This approach does not give precise stability boundaries for asymmetric traps, but it is "safe" in the sense that trap operating conditions deemed stable by this method will in fact be stable for the coupled system. By ignoring the coupling, the size of the primary stability region is simply underestimated.

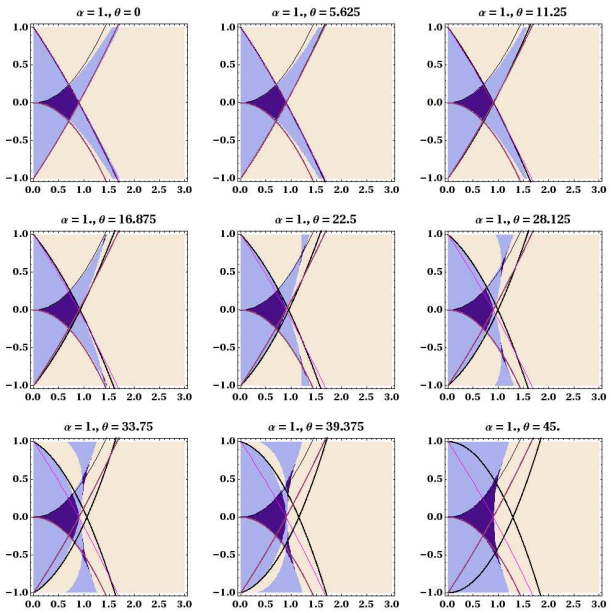

Figure 14: Stability plots for $\alpha = 1.0$ and θ between $0°$ and $45°$, with a step size of $5.625°$. See the caption for Figure. 13.

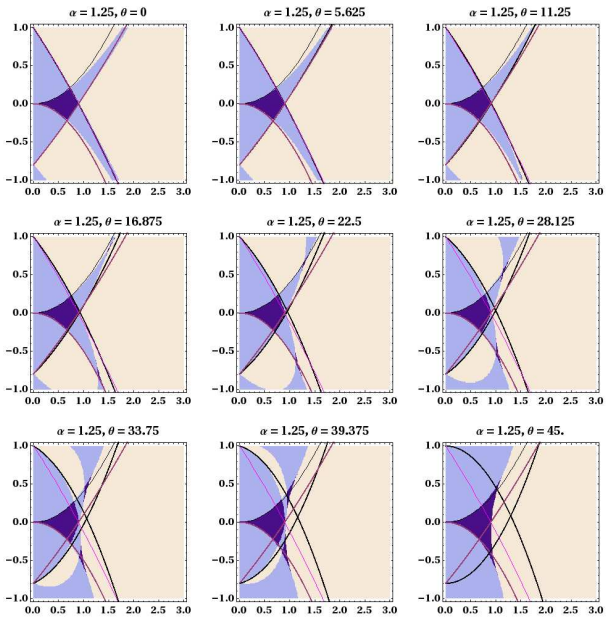

Figure 15: Stability plots for $\alpha = 1.25$ and θ between $0°$ and $45°$, with a step size of $5.625°$. See the caption for Figure. 13.

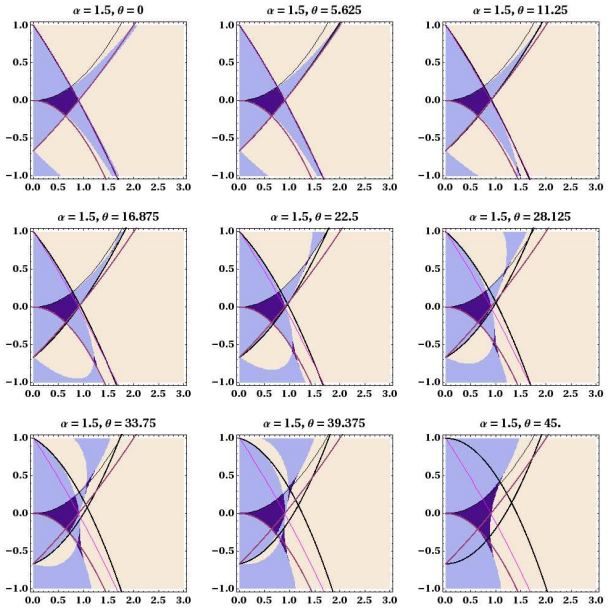

Figure 16: Stability plots for $\alpha = 1.5$ and θ between $0°$ and $45°$, with a step size of $5.625°$. See the caption for Figure. 13.

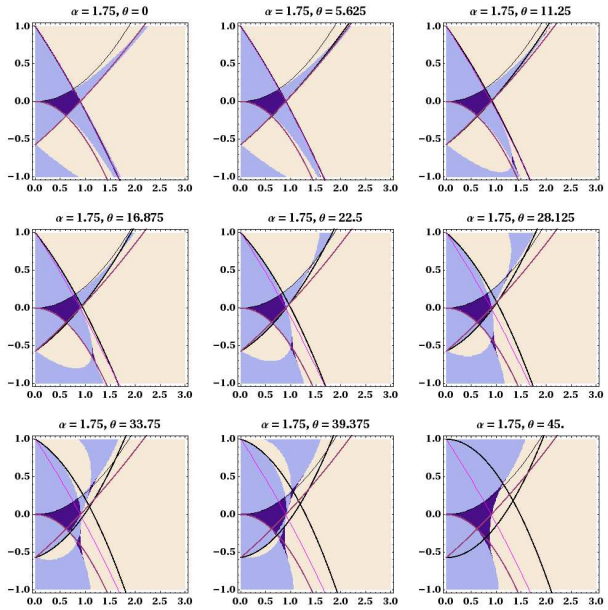

Figure 17: Stability plots for $\alpha = 1.75$ and θ between 0° and 45°, with a step size of 5.625°. See the discussion under Figure. 13.

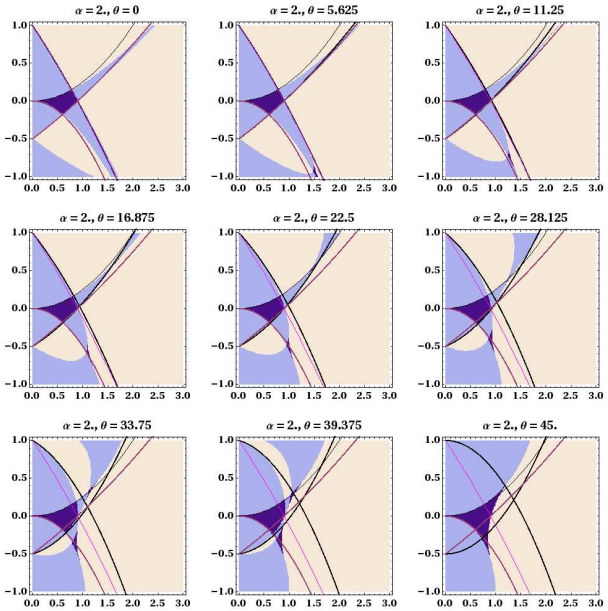

Figure 18: Stability plots for $\alpha = 2.0$ and θ between 0° and 45°, with a step size of 5.625°. See the discussion under Figure. 13.

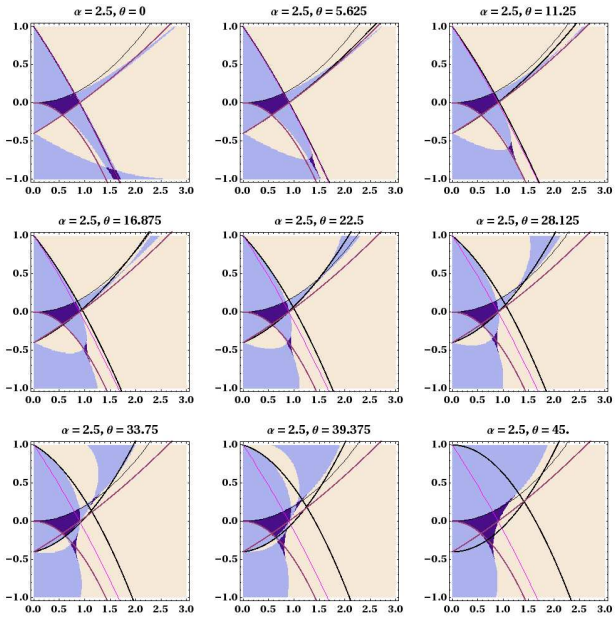

Figure 19: Stability plots for $\alpha = 2.5$ and θ between $0°$ and $45°$, with a step size of $5.625°$. See the discussion under Figure. 13.

CHAPTER 5

MONOLITHIC SYMMETRIC ION TRAP : DESIGN

5.1 Motivation

A number of experiments and proposals that use linear chains of ions to simulate quantum systems or to perform quantum computation have recently been developed [1-4]. The ions are entangled through the modes of their collective motion, either by applying an optical spin-dependent force [51, 81, 21] or through an alternating magnetic field gradient [82]. A quantum simulation of the Ising model subject to a transverse magnetic field has been performed on three ions held in a linear RF trap, coupled through the transverse motional modes. This three-ion system was scaled to large numbers of ions by confining the ions in an anharmonic linear potential with nearly equal spacing between them [51]. If the trap can be designed to hold thirty ions or more in a stable linear chain, it should be possible to study quantum systems that cannot be currently simulated using classical methods. Trapping long ion-chains places a number of significant demands on the trap performance. For instance, generating an anharmonic potential for equally spaced ions requires a large number of segmented electrodes [83]. While it is possible to approximate this potential using as few as five electrode pairs maximizing inter-ion spacing uniformity, it could require as many as ten pairs of electrodes for longer chains [51]. The microfabricated surface-electrode ion traps offer the flexibility of having many electrodes in different configurations and the scalability that is required to trap multiple ions. However, surface-electrode traps have lower trapping depths and larger anharmonic terms in the radial trapping potential compared to traditional four-rod Paul traps. These characteristics can result in reduced ion lifetimes and increased mode frequency drift. Both of these issues become more important as the system is scaled-up for multiple ions. The two-level and three-level ion traps (discussed in Chapter 3), on the other hand, have larger trapping depths and can provide the symmetry in radial fields that are helpful in trapping longer ion chains. However, designs that have been demonstrated

to date, have dimensions that are on the order of hundreds of microns resulting in reduced control granularity and undesired non-uniformities in long ion-chain spacings.

The trap design proposed in this chapter features a novel structure that can be fabricated using processes similar to those used for microfabricated surface-electrode ion traps. The trap structure is a hybrid of surface-electrode and two-level structures. It provides the benefits of the surface-electrode traps such as the flexibility in electrode configuration and scalability of microfabrication in addition to the benefits of two-level traps such as deeper and symmetric trapping potentials. Numerical electrostatic simulation studies of the proposed trap design indicate that the trap has an order of magnitude deeper radial-trapping potential and reduced radial anharmonicities in the RF confinement field as compared to that of surface-electrode traps. It is expected that the larger trap depth will increase ion-chain lifetimes and the reduced radial anharmonicities will suppress mode frequency drifts associated with dielectric charging. This trapping structure, therefore, combines the flexibility and scalability of silicon microfabrication technologies with the superior trapping characteristics of traditional four-rod Paul traps.

5.2 Overview

A cross-section of the new design is shown schematically in Figure 20. The ion is trapped nearly symmetrically between two red electrodes (shown in Figure 20) that are biased with RF voltages. The trap depth is near 1 eV for $^{171}Yb^{+}$ ion, approximately 20 times larger than the depths typically obtained for the surface-electrode traps with similar dimensions. Ion-chain lifetimes are likely to scale with the trap depth, optimizing the chances for success in the QIP experiments with long chains. The symmetric trap also provides a reasonably large central slot, 125 μm wide, for good optical access that should result in minimal light scattering and photoemission from the nearby electrodes. The symmetric potentials near the trapped ion location may also aid in stabilizing the ion motion by avoiding anharmonic terms that can destabilize the ion radial motion.

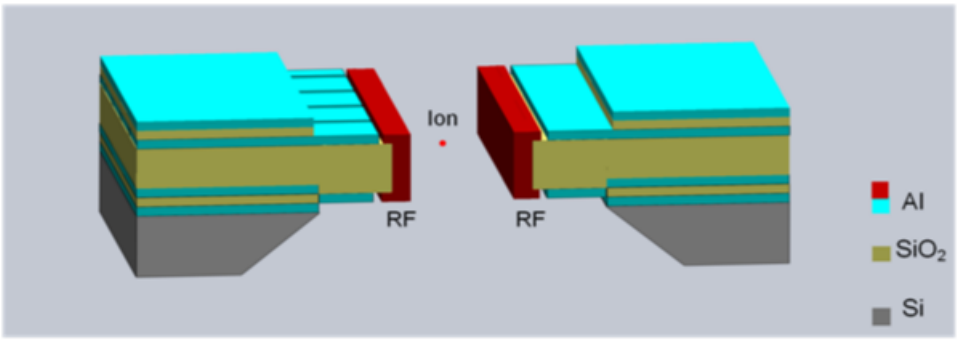

Figure 20: Symmetric trap cross-section (not to scale). The RF electrodes are in red and the DC control electrodes and ground electrodes are in blue. The SiO_2 dielectric is in yellow. The highly doped silicon substrate is in dark grey.

The beveled sides of the central slot provide through-chip optical access. They can be formed by etching the Si substrate using pottasium hydroxide (KOH). The dimensions of this slot were chosen to be as large as possible to reduce light scattering and consequent photoemission but not so large as to require excessively large RF and control voltages to maintain adequate trap depth. For example, if the slot width were increased to 200 μm , the RF peak potential would have to be well above 300 V to maintain a 1 eV trap depth for $^{171}Yb^{+}$ ions at 40 MHz RF frequency. This potential is more likely to cause arcing from the RF electrode to nearby RF grounds. However, for a 125 μm slot the trap depth is about 1 eV for only 180 V applied RF. A trap depth of 1 eV is an order of magnitude larger than the depths typically obtained for surface-electrode traps of similar size. Furthermore, the symmetric structure of the trap is expected to aid in stabilizing the radial-mode frequencies by avoiding anharmonic terms in the RF pseudopotential that are present in surface-electrode traps. The gap between electrodes is chosen to be 5 μm . This gap keeps the exposed oxide to a minimum while maintaining a large enough gap to prevent RF arcing. The metallic layers are all 1 μm thick aluminum (Al). The ground electrodes overlaying the DC control electrodes provide a capacitive RF short to ground, minimizing any RF pick up on the control electrodes. This upper ground layer also protects the top electrodes from scratches. A 1 μm thick dielectric (SiO_2) layer separates this ground from the control electrodes. The DC control electrodes are segmented in 60 μm wide sections, as shown in Figure 21(b).

The alternate diagonals are single long unsegmented electrodes that can be biased to aid in compensating the trap and controlling the angle of the principal axes for the ion motion. We conducted a study of the effects of the DC electrode segmentation scheme on the radial trapping depth of the trap and found that the diagonal segmentation scheme not only gives a slight improvement in the radial trapping depth but also keeps the required DC potentials under experimentally limited values (< 10 V). The results of the effects of different segmentation schemes on radial depth and the required DC potentials values are listed in the Table 1.

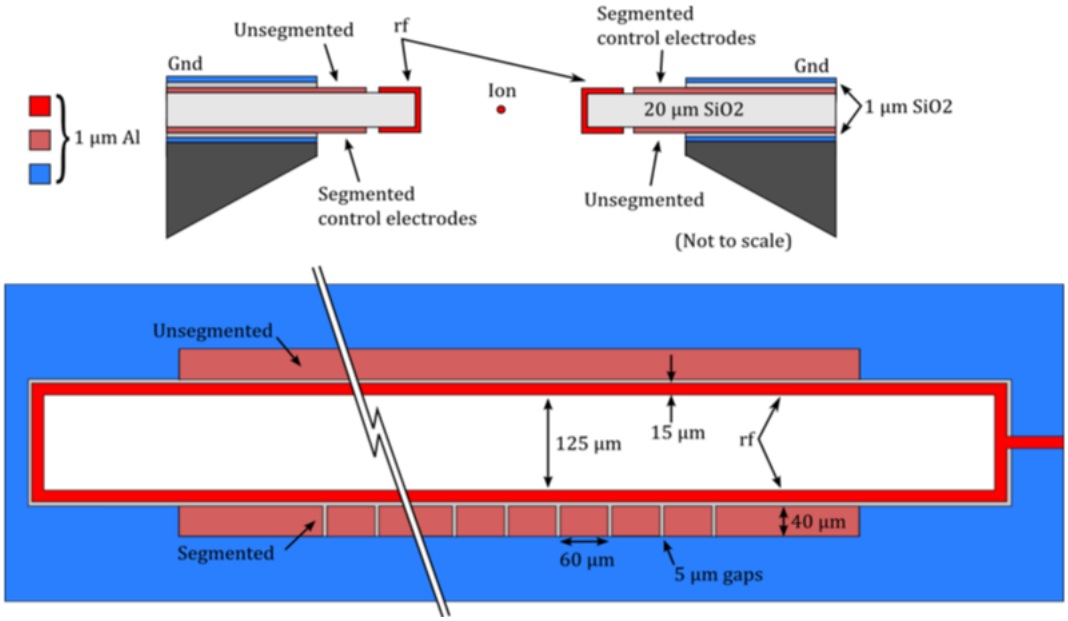

Figure 21: Side (above) and top (below) view of the symmetric trap showing dimension details. The ground plane above the top electrodes defines the control voltages and protects the upper electrodes from damage.

Although leaving two of the diagonal electrodes unsegmented somewhat restricts the control of the ion-chain, it keeps the required number of electrode connections to below 50 (based on the available hardware) and consequently simplifies the in-vacuum hardware needed to mount this trap. The set back of the DC electrodes from the RF electrode faces is 20 μm (15 μm RF width plus 5 μm gap). This is a critical dimension for the design and must be kept to a minimum; otherwise, the DC control voltages required to trap the chain exceed 20 V. The effect of DC setback for different RF rail widths on the lower and bottom faces of

the trap on the radial trapping depth is shown in Table 2(a). From the fabrication standpoint the RF rail width has to be wide enough to avoid contact photolithographic errors. An RF rail width of 15 μm (DC setback of 20 μm) keeps the radial depth large enough and meets the fabrication critical dimension criterion.

The thick 20 μm oxide layer that forms the vertical face of the RF rail, provides a large trap depth for only 250V applied RF peak (1.14 eV at 60 MHz RF frequency for $^{171}Yb^{+}$) and also contributes to the mechanical stability of the structure. Simulation studies show that reducing the oxide thickness to 10 μm will result in only a 20 % reduction in trap depth but may physically weaken the structure. The stability of the trapping frequencies is an important consideration for experiments using microfabricated ion traps since charging of nearby exposed insulators can affect these frequencies. The oxide thickness effects on the radial depth are shown in Table 2(b). The proposed symmetric-trap design does not have a line-of-sight from the ion to any of the exposed oxide, reducing the influence of charges on these surfaces [84]. Compared to surface-electrode traps, the high symmetry in this design reduces anharmonicities in the radial pseudopotential and consequently reduces the dependence of the radial mode frequencies on stray fields created by the charging. A top shield is used to shield ion from the stray fields. A study of the top shield effects on the radial trapping depth are shown in Table 2(c). This study suggests no significant variation in the trapping depth due to the presence of the top-shield. This allows the top-shield to be designed with increased optical access. Various top-shield designs for this traps are discussed in Chapter 7.

Table 1: Comparative analysis of the segmentation schemes of the DC electrodes against radial trap depth and DC potentials required to trap single $^{171}Yb^{+}$ ion at the RF peak voltage of 250 V and RF frequency of 60 MHz.

	DC electrodes segmented on all sides	**DC electrodes segmented on top sides**	**DC electrodes segmented on diagonally opposite sides**
Radial trap depth (eV)	1.075	1.145	1.366
Absolute peak voltages (V)	3.7	10.7	9.3

Table 2: Comparative analysis of various dimensions of the trap design against the radial trap depth using BEM model. The trap depths are calculated for $^{171}Yb^{+}$ ion with peak RF voltage of 250 V and RF frequency of 60 MHz.

(a) The effect of various DC setbacks (RF rail width plus RF-DC gap) on the radial trap depth.

DC Setback(μm)	Radial Trap Depth (eV)
5	1.323
10	1.316
15	1.292
20	1.251
25	1.154

(b) The effect of different oxide thicknesses on the radial trap depth.

Oxide Thickness (μm)	Radial Trap Depth (eV)
10	0.971
15	1.085
20	1.141
25	1.186
30	1.154

(c) The effect of the top-shield (discussed in Chapter 7) distance from the surface of the trap on the radial trap depth.

Shield Distance (mm)	Radial Trap Depth (eV)
0.5	1.31
1.5	1.277
2	1.276

Optical access for the cooling, photoionization, and gate beams is one of the primary considerations in trap design. The slot opening of 125 μm provides enough room for the beams entering and exiting axially as well as radially. A 3D view from the back side of the trap chip is shown in Figure 22. The trap can be mounted in the UHV chamber so that the slot's longer dimension is horizontal or vertical (see Chapter 7 for UHV apparatus details) due to its generous optical access. For the vertical slot orientation, Raman laser beams traverse through the slot in a horizontal plane and impinge on the ions from opposite sides of the trap so that the difference in laser beam momenta excites the horizontal radial mode. The beveled slot sides allow these beams to enter at an angle of up to 40° with respect to the normal to the trap plane so that the radial modes can be excited. The access is only

limited by the in-vacuum socket components and not by the trap structure.

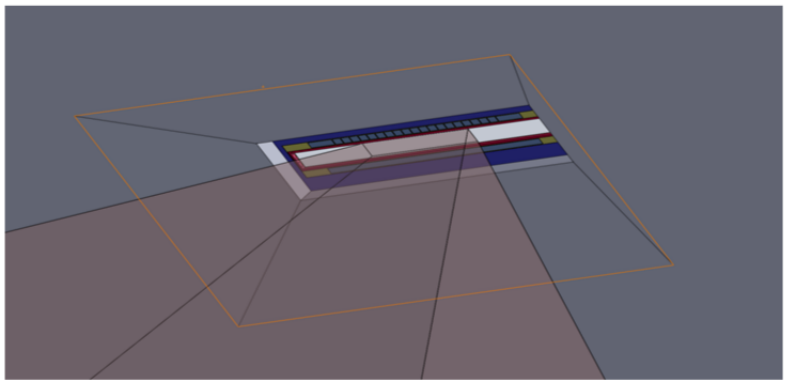

Figure 22: A 3D view of the back of the symmetric trap outlining the optical access and showing the KOH etched silicon wafer (orange outline on the lower wafer surface). The silicon wafer is approximately 500 μm thick.

Because of the robustness of the design of this trap modifications that simplify fabrication can easily be made in the design without impacting the trap depth and other inherent characterisitics of this trap design. The trap cross-section is slightly modifed from the cross-section shown in Figures 20 and 21, to further simplify the fabrication process. The new cross-section of the trap is shown in Figure 23. The top DC electrodes are connected to the bottom DC electrodes layer through on-chip vias. Behind the bottom layer DC electrodes, new via pads are added which act as fan-out for the top DC electrode layers. The following discussion and simulation results correspond to the cross-section shown in Figure 23

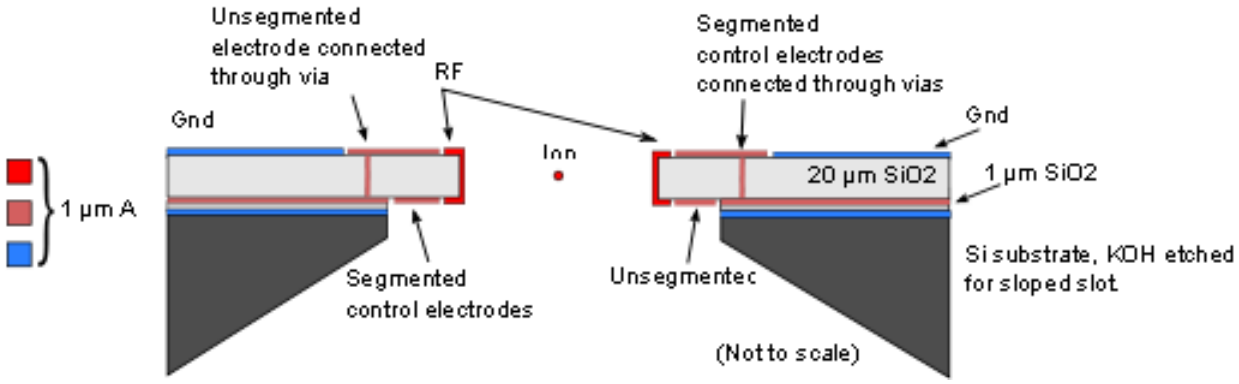

Figure 23: Slightly-modified cross-section of the symmetric-trap design. Top DC electrodes are connected through via pads to the bottom layer. This modification makes the trap fabrication simpler.

5.3 Single $^{171}Yb^{+}$ ion simulations

An extensive set of simulation software is available at Georgia Tech Research Institute (GTRI) for ion trap modeling. In this software, an efficient method of moments (MoM) code is used to find the electrostatic fields that result from complex trap-electrode geometries. The three components of the electric field, E_x, E_y, E_z, and the voltage, V_x, V_y, V_z, resulting from each electrode are compiled in a data-cube. These fields are then combined and weighted by applied voltages to the various electrodes. Initially, a single ion-trapping well is analyzed using a MatLab program. In this case three central DC electrodes form the required axial-trapping potential. Typical single ion trapping characteristics are shown as a color map of the total potential in Figure 24. The radial-trapping potential for a peak of 180 V RF at 40 MHz RF frequency is shown in Figure 24(a). The combined RF pseudo-potential and DC-control potentials are shown in Figure 24(b). The geometric trap center is at $x = y = 0$. Note that the ion is trapped at the potential minimum in close proximity to the geometric trap center. The trap parameters for this case listed below:

- Segmented top DC electrode voltages (V): 2.72, -14.19, 2.72,
- Segmented bottom DC electrode voltages (V): 1.93, -13.79, 1.93,
- Unsegmented top and bottom electrode (V) : 0, 0,
- RF peak voltage (V): 180,
- RF Frequency (MHz): 40,
- RF electrode DC bias (v): -3,
- Radial mode frequencies (MHz): 4.8, 5.8, 1.0,
- Angle rotation of radial modes: 11°,
- Total radial well depth is 1.15 eV.

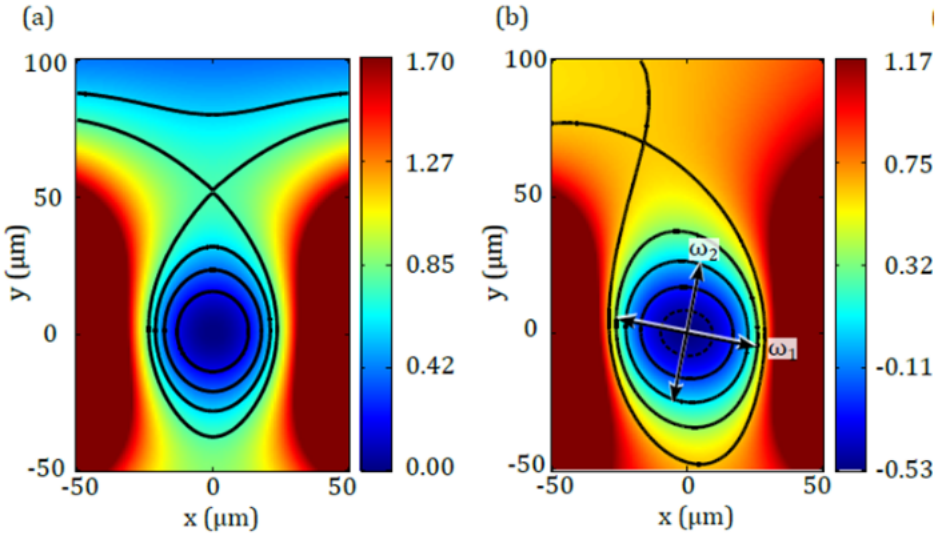

Figure 24: A single $^{171}Yb^{+}$ ion trapping potentials.(a) Radial trapping potential for a peak 180 V RF potential at 40 MHz RF frequency. The radial trap depth is 0.76 eV, which corresponds the self-intersecting equipotential curve. The ion is trapped at $x = y = 0$. (b) Total radial potential including the DC potentials.

The axial modes in this case are split by 1.0 MHz by using a -3 V DC bias on the RF rails. For this simulation case, the DC voltages are higher than the typical values of 5 to 10 V. Even though the substrate is cut back and there is an angled-slot on the back that is grounded. This causes the small asymmetry in the trapping potential.

5.4 Single $^{40}Ca^{+}$ ion simulations

A single $^{40}Ca^{+}$ ion trapping potentials for the symmetric trap are calculated. These potentials are calculated to use three central segmented DC electrodes. A single $^{40}Ca^{+}$ ion trapping characteristics are shown as a color map of the total potential in Figure 25. The radial-trapping potential for a peak of 60 V RF at 40 MHz RF frequency is shown in Figure 25(a). The combined RF pseudo-potential and DC-control potentials are shown in Figure 25(b). The geometric trap center is at $x = y = 0$. The trap parameters for this case listed below:

- Segmented top DC electrode voltages (V): 0.638, -3.3, 0.638,

- Segmented bottom DC electrode voltages (V): 0.459, -3.21, 0.459,
- Unsegmented top and bottom electrode (V) : 0, 0,
- RF peak voltage (V): 60,
- RF Frequency (MHz): 40,
- RF electrode DC bias (v): -3,
- Radial mode frequencies (MHz): 6.0, 8.9, 1.0,
- Angle rotation of radial modes: -178°,
- Total radial well depth is 0489+0.053=0.542 eV.

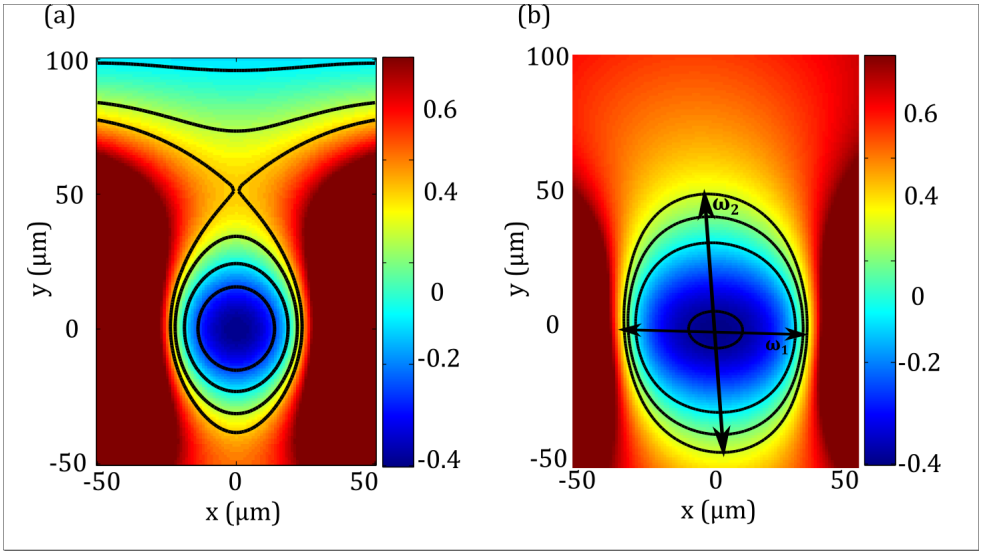

Figure 25: A single $^{40}Ca^{+}$ trapping potentials. (a) Radial trapping potential for a peak 60 V RF potential at 40 MHz RF frequency. The radial trap depth is 0.496 eV, which corresponds the self-intersecting equipotential curve. The ion is trapped at $x = y = 0$. (b) Total radial potential including the DC potentials.

5.5 Linear ion chain simulations

The potentials to trap ion-chains are optimized by an algorithm that uses many degrees of freedom of the electrode structure and voltages to obtain, (1) equal ion spacing, (2) equal principal-axis rotation for each ion, (3) precision compensation for each ion in the chain,

and (4) constant curvature of the transverse field at each ion location. A potential map for a 20 ion-chain obtained using this algorithm is shown in Figure 26.

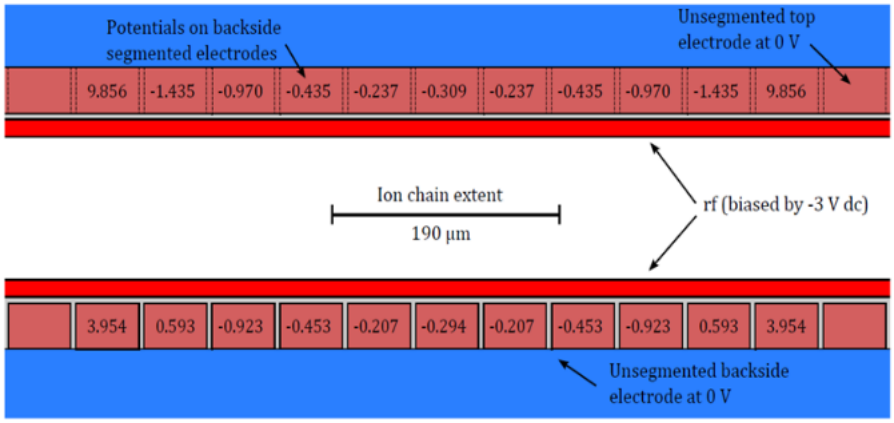

Figure 26: (a) Top schematic view of the symmetric trap is shown along with the segmented control-electrode voltages optimized for equal spacing of 10 μm of a 20 ion-chain.

The mode spectrum for this 20 ion-chain is shown in Figure 27. The relatively large spacing between the radial modes is required for quantum simulation experiments. The mode spectrum is obtained by using an ion motion solver and then by applying the Fourier transform on the ion motion [85].

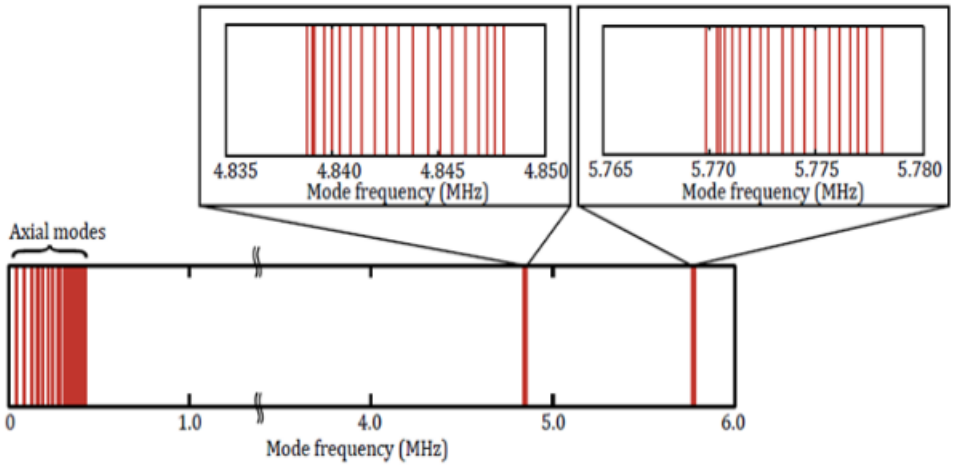

Figure 27: Mode spectrum for a chain under the potentials for $^{171}Yb^{+}$.

Deviations from equal ion spacing along the chain and deviations from equal principal axis orientation are shown in Figure 28. These deviations ($< 1\mu m$) are within the error boundaries of the requirements of a successful linear-chain quantum simulation experiment [85].

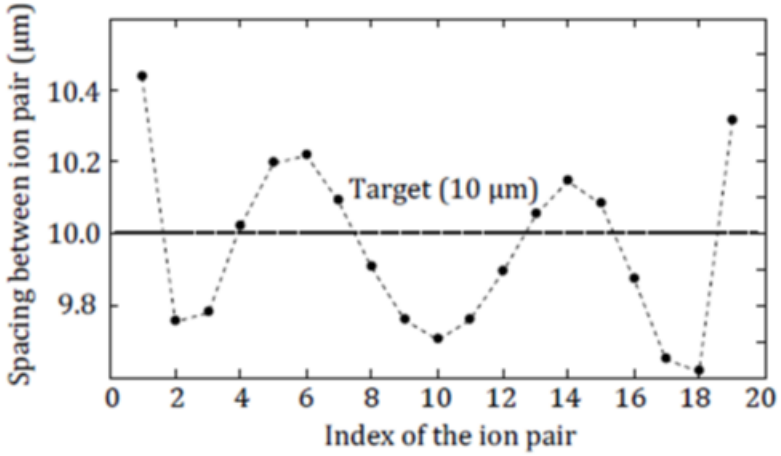

Figure 28: Deviations from equal ion spacing across the 20 ion-chain.

The effect of DC electrode width on the ion chain control has been studied for 20-ion chain and 50-ion chain of $^{171}Yb^{+}$ ions. From the results shown in Table 3, it appears that decreasing the electrode width beyond 60 μm gives no additional benefit. However, it can be concluded that the improved control of ion spacing, principal axis orientation, and compensation are obtained by increasing the number of control electrodes and decreasing the electrode width to this limiting value.

Table 3: Spacing errors as a function of electrode width for (a) 20 and (b) 50 ion chains of $^{171}Yb^{+}$ ions. The target ion spacing is 10 μm for both cases.

(a) 20 ion chain with 10 μm spacing			
Electrode width (not including 5 μm gaps)	500 μm	60 μm	30 μm
No. of active electrodes	5	5	7
Max. spacing error	4.7 μm	0.75 μm	0.65 μm

(b) 50 ion chain with 10 μm spacing			
Electrode width (not including 5 μm gaps)	500 μm	60 μm	30 μm
No. of active electrodes	5	7	10
Max. spacing error	12 μm	1.5 μm	1.6 μm

CHAPTER 6

MONOLITHIC SYMMETRIC ION TRAP : FABRICATION

The focus of this thesis is a novel symmetric trap. A cross-section of the trap is shown in Figure 23. It is fabricated in the Nanotechnology Research Center (NRC) at Georgia Tech. Many surface-electrode trap designs have been built by the QIS group in GTRI [75] using standard Si-based fabrication technologies. Experience gained from the fabrication of these surface-electrode traps were incorporated in designing the fabrication process-flow for the symmetric trap. Since the symmetric trap design has a membrane structure, several new processes had to be developed that are specific to the requirements of this trap design.

Two generations of the symmetric traps were built successfully between September 2010 and April 2012. During the development of processes and fabrication of the symmetric trap, several substrate samples were processed. This chapter presents the process steps for two generations of trap. Generation **A** represents the traps that were tested between Oct 2011 and Jan 2012. Generation **B** represents the traps that were tested between April 2012 and September 2012. There is no cross-sectional difference between the two trap generations. The differences between generation **A** and **B** traps are discussed in the following sections along with the discussion of the fabrication steps and choice of materials.

Cross-section of the 3D CAD model of the trap is shown in Figure 29. In this figure all metallic and dielectric layers are identified in blue and yellow respectively. Layers identified with *M1, M2, M4* are metal layers used as either ground, active conductive layer, or a mask. Layers identified as *D1, D2* are two SiO_2 dielectric layers used as insulators.

6.1 Materials

The trap structure is built from the metal, dielectric, and semiconductor materials. The metal must be highly conductive, non-corrosive, non-magnetic, smooth, compatible with

high temperature ~ 200°C, ultra high vacuum (UHV), and Si-based fabrication technologies. Lithographic processes are used in the fabrication so that the metal is patterned and adhered to either substrate or the dielectric material. Due to successful demonstrations of the Al-based surface-traps [86], this symmetric trap also uses Al as the conductor. In VLSI technology, Al has emerged as preferred metal because it avoids the problems of high contact resistance and havocs as compared to Copper. Al has low resistivity of 2.7 $\mu\Omega$-cm, slightly higher than Cu and can withstand high current density [87].

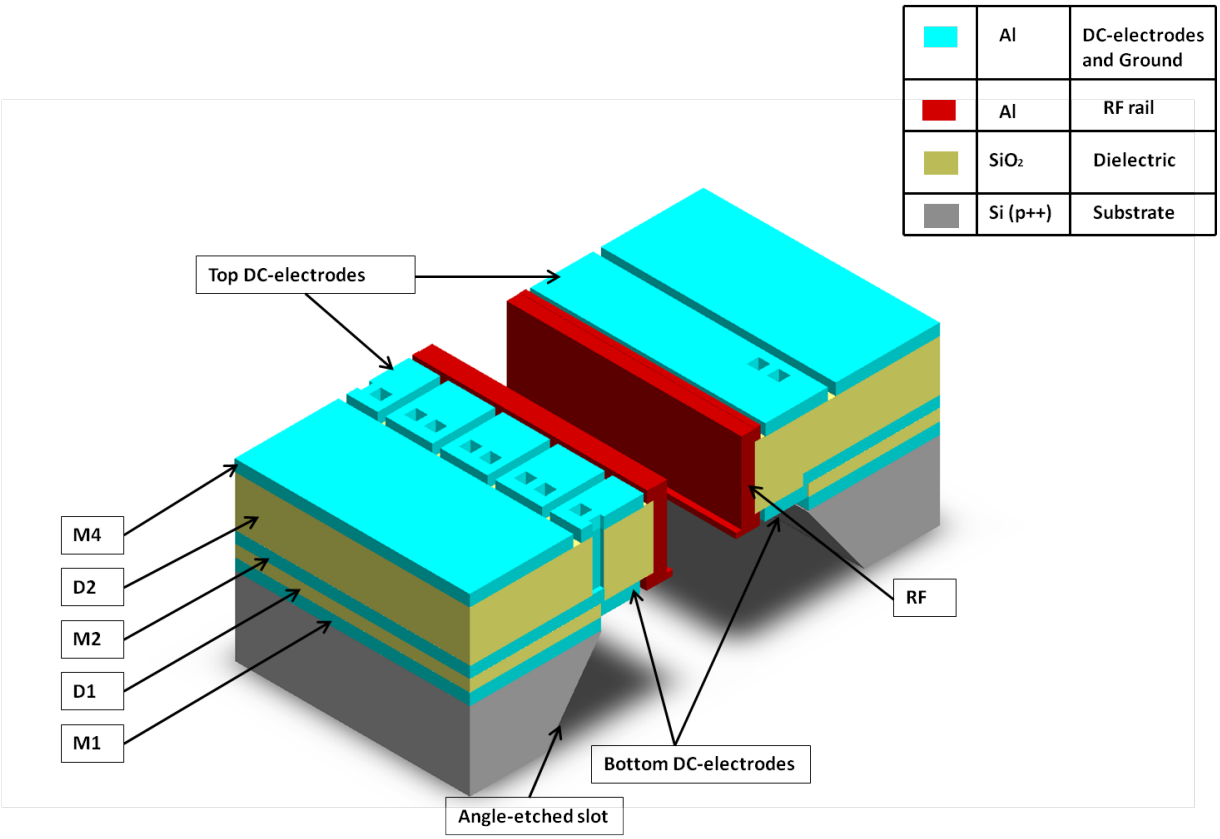

Figure 29: 3D drawing of the symmetric trap. The drawing identifies all the metallic and dielectric layers deposited as structure is bulti up.

The properties of Al material including adhesion to silicon dioxide, availability in high purity, naturally low contact resistance with silicon, and ease of patterning with conventional photolithography processes, make it the primary choice for the symmetric trap conductor material. In VLSI technology it is common to add impurities to the Al ($\sim 1\% - 4\%$) to avoid the problems caused by electromigration. With the heat generated by the high

current through Al leads, the Al diffuses within itself causing electromigration. Adding the impurities such as Si, Cu, and Ti avoids this problem. Additionally, to avoid the problems of eutectic formation between Al and Si interface, a Ti adhesion conductive layer is typically used between Al and Si. This layer serves two purposes: it provides adhesion and it avoids the dissolution of Al and Si. For the symmetric trap the conductive layers are made of Al (1% Si) for generation **A** traps and Al (1% Cu) for generation **B** traps. A 600 Åthick layer of Ti is used as an adhesion layer.

Silicon dioxide (SiO_2) is used for the dielectric layer. SiO_2 has many advantages and it is the most popular dielectric in semiconductor industry. Apart from its dielectric properties, SiO_2 is preferred due to its surface passivation, its ease of growth with low contaminants (or particles), its hardness, and ease of stress control. SiO_2 patterning or etching is also a well-controlled reaction. For RF applications, SiO_2 has the important advantage of a low tangent-loss factor (~ 0.001), low-loss ion traps.

Since the trap structure has a metallic ground layer on top of the Si substrate. This metallic layer makes shields the substrate from RF fields. Without this ground shield the RF losses in the Si substrate would be far too large. Heavily boron-doped p++ $< 100 >$ Si with resistivity of $0.02\ \Omega - cm$ is chosen as a substrate material. During the initial steps of the structure build-up, the Si has to be wet-etched. Silicon nitride (SiN) is used as mask to protect the areas that are to be kept from etching during this wet-etch process. Details of the processes and steps are discussed in the following sections.

6.2 Processes

Like any standard Si-based fabrication device, this trap is fabricated using three main process categories, deposition, etching and photolithography. For deposition, plasma enhanced vapor deposition (PECVD), low pressure chemical vapor deposition (LPCVD), and physical vapor deposition (PVD) or RF sputtering is used (See Table 4). For etching, several wet-etch recipes have been developed to remove metal, oxide, and residue films. These

recipes are often used in combination with dry etching processes. Dry etching processes include reactive ion etching (RIE) and inductively coupled plasma (ICP) etching. RIE processes are used to etch metal, oxide, and Si. In addition to using RIE/ICP and wet-etching processes, a chemical-mechanical polishing (CMP) process is used to remove and planarize SiO_2 . Photolithography involves spin-coating of photo-resist, UV-light exposure, and development steps. All photolithography is performed with negative photo-resist. The masks are designed according to negative photolithography recipes. The deposition and etching process recipes and parameters are given in the Tables 5, 6, 7, and 8. The recipes and parameters for the contact photolithography are given in Table 9. The detailed process flow to build this trap consists of the processes given in these tables and some additional steps that are given in Table 6.3.

Table 4: List of materials and proccesses used in the fabrication of the symmetric trap.

Material	Layer	Deposition	Dry etch	Wet etch
Al(Si)/Al(Cu)	Conductor and ground	RF Sputtering	RIE/ICP	Al etchant type A
Ti	Adhesion	RF Sputtering	RIE/ICP	EGBOE*
SiO_2	Insulator	PECVD	ICP	EGBOE
Si	Subsrtate	-	ICP(Bosch)	KOH**(25%)
SiN	Mask	LPCVD	RIE	HF(49%)

* Ethylene Glycol Buffered Oxide Etch

** Potassium Hydrogen Peroxide

6.3 Process flow

In this section, each fabrication process step is described in detail. The process flow steps are listed in Table 6.3. The 3D model of the ion-trap structure and its build-up as each process step completes, is shown in Figure 43. The structure is built-up by following the cycle of desposition of a material using a recipe from Table 5, contact lithography using a recipe from Table 9, etching the material by a combination of recipes from Tables 6, 7, and 8, and finally stripping the photo-resist to clean up the residue from lithographic process. The cleaning recipes are one of the key components of the fabrication process. Residue left after incomplete clean can cause variety of problems, ranging from peel-off

Table 5: Deposition process recipes used in the fabrication of the symmetric trap.

Material	Tool	Deposition rate	Recipe
Al(Si)/Al(Cu)	Unifilm sputterer	600 Å/m	Ar flow: 90 sccm RF current: 0.09 A RF Voltage: 1.05 V
Ti	Unifilm sputterer	100 Å/m	Ar flow: 90 sccm RF current: 0.18 A RF Voltage: 1.34 V
SiO_2	Unaxis PECVD	560 Å/m	Temp: 250°C N_2O : 900 sccm SiH_4: 400 sccm with 5% He RF Power: 25 W Process pressure: 900 mTorr
SiN	Trystar LPCVD furnace	40 Å/m	Temp: 835°C H_2SiCl_2: 100 sccm NH_3: 17 sccm Process pressure: 130 mTorr

Table 6: Dry-etch process recipes used in the fabrication of the symmetric trap.

Material	Tool	Etch rate	Recipe
Al(Si)/Al(Cu)	Plasma-Therm ICP	250 Å/m	BCl_3 flow: 10 sccm Cl_2 flow: 30 sccm Process pressure: 10 mTorr RF1 power: 180 W RF2 power: 400 W
Ti	Plasma-Therm ICP	200 Å/m	BCl_3 flow: 10 sccm Cl_2 flow: 30 sccm Process pressure: 10 mTorr RF1 power: 180 W RF2 power: 400 W
SiO_2	Plasma-Therm ICP	560 Å/m	CF_4 flow: 45 sccm O_2 flow: 10 sccm Process pressure: 8 mTorr RF1 power: 6 W RF2 power: 800 W
SiN	Vision RIE	314 Å/m	Temp: 25°C CHF_3 flow: 45 sccm O_2 flow: 5 sccm Process pressure: 40 mTorr RF power: 270 W
Si	Plasma-Therm ICP	1.2 μm /m	See Table 7
Photo-resist O_2 plasma descum	Vision RIE	-	O_2 flow: 500 sccm Process pressure: 310 mTorr RF power: 250 W
Metal native oxide Ar plasma descum	Vision RIE	-	Ar flow: 60 sccm Process pressure: 60 mTorr RF power: 350 W

Table 7: Si dry etch process recipe parameters. The process is known as Bosch process. Apart from the standard process steps, this process has additional three steps : one deposition step and two etch steps in a cycle. Deposition step deposits the carbon to protect the side-walls to achieve an isotropic plasma etch. This recipe is used to etch isotropic Si on Plasma-Therm ICP tool. Each cycle etches 0.65 μm of Si.

Parameter	Deposition	Etch A	Etch B
CF_4 (sccm)	70	0.5	0.5
SF_6 (sccm)	0	50	100
Ar (sccm)	40	40	40
Process pressure (mTorr)	15	15	15
RF1 power (W)	1	9	12
RF2 power (W)	800	800	800
Time (sec)	4	2	16

of the thin films, high-resistance contacts, de-laminating films, and defective insulation characteristics.

Table 8: Wet-etch process recipes used in the fabrication of the symmetric trap.

Material	Etch rate	Recipe
Al(Si)/Al(Cu)	200 Å/m	Al etchant type A
Ti	75 Å/m	EGBOE
SiO_2	1000 Å/m	EGBOE
SiN	35 Å/m	HF(49%)
Si	1 μm /m	KOH(25%) at 80°C

Table 9: Contact photolithography recipes used in the fabrication of the symmetric trap

Phot-resist (PR) = Shipley 1827
Developer = MF-319

Step	Process	Litho SiN	Litho M1	Litho M2	Litho Via mask	Litho M4
		SiN etch	Al(Si)/Al(Cu) etch	Al(Si)/Al(Cu) etch	Al(Si)/Al(Cu) etch	Al(Si)/Al(Cu) etch
1	HMDS coat spin*	1000/500/10	1000/500/10	1000/500/10	1000/500/10	1000/500/10
2	PR spin 1 *	1000/500/10	1000/500/10	1000/500/10	1000/500/10	1000/500/10
3	PR spin 2 *	3000/1000/40	3000/1000/40	3000/1000/40	3000/1000/40	1000/1000/40
4	Soft bake (temp/time)	115°C/ 12 m	115°C/ 12 m	115°C/ 12 m	115°C/ 12 m	115°C/ 12 m
5	Exposure	800 mJ/cm^2	500 mJ/cm^2	500 mJ/cm^2	500 mJ/cm^2	600 mJ/cm^2
6	Development time	4 m	4 m	4 m	4 m	4 m
	Photo-resist thickness	4 μm	4 μm	4 μm	4 μm	6 μm

* Spin recipes in target/ramp/time in rpm/rpm/s

Table 10: Process flow of the symmetric trap fabrication. Corresponding deposition, etching, and photolithogrpaphic recipes and parameters are given in Tables 5, 6, 7, 8, 9.

Step	Process Step Name	Equipment	Recipe
1	Scribe wafer ID		
2	Wet-clean wafer	CMOS wet bench and Spin Dryer	1. Pirranha (3:1::H_2SO_4:H_2O_2) soak @ 120°C for 10 m 2. Rinse with water for 5 m 3. BOE (6:1) Soak for 10 s 4. Rinse with water for 5 s 5. Dry in spin dryer for 30 s
3	Deposit SiN	Tystar Nitride Furnace	See Table 5
4	Litho SiN	MA-6 Mask Aligner	See Table 9
5	Dry etch SiN	Vision RIE	See Table 6
6	Strip photo-resist	Vision RIE	1. Rinse with Acetone 2. Sonicate in Acetone for 2 m 3. Rinse with IPA 4. O_2 plasma descum for 10 m
7	Wet etch Si (back side slot)	MEMS Wetbench	$\sim$ 400 μm etch - See Table 8
8	Wet etch SiN	MEMS Wetbench	See Table 8
9	Wet-clean wafer	MEMS Wetbench	BOE (6:1) Soak for 10 s and rinse with water for 5 m
10	Deposit M1 (Ti + Al(Si)/Al(Cu))	Unifilm Sputterer	1. Deposit Ti 600 Å- See Table 5 2. Deposit Al(Si) or Al(Cu) 3000 Å- See Table 5
11	Measure sheet resistance	Signatrone 4-point probe	
12	Litho M1	MA-6 Mask Aligner	See Table 9
13	We etch M1 (Al(Si)/Al(Cu))	Wet Etching	See Table 8
14	Strip photo-resist	Vision RIE	1. Rinse with Acetone 2. Sonicate in Acetone for 2 m 3. Rinse with IPA

Continued on Next Page...

Table 10 – Continued

Step	Process Step Name	Equipment	Recipe
			4. O_2 plasma descum for 10 m
15	Measure metal thickness	KLA-Tencor P15 Profilometer	
16	Deposit D1 SiO_2	Unaxis PECVD	1 μm SiO_2 using recipe in Table 5
17	Measure oxide thickness	Nano-spec Refractometer	
18	Deposit M2 (Ti + Al(Si)/Al(Cu))	Unifilm Sputterer	1. Deposit Ti 600 Å- See Table 5 2. Deposit Al(Si) or Al(Cu) 1 μm - See Table 5
19	Measure sheet resistance	Signatrone 4-point probe	
20	Litho M2	MA-6 Mask Aligner	See Table 9
21	Etch M2	Plasma Therm ICP	1. Wet etch for 15 m - See Table 8 2. Dry metal etch - See Table 6
22	Strip photo-resist	Vision RIE	1. Rinse with acetone 2. Sonicate in acetone for 2 m 3. Rinse with IPA 4. O_2 plasma descum for 10 m
23	Measure metal thickness	KLA-Tencor P15	Metal step height
24	Electrical test	Probe Station	Probe test wirebonding pads to test for shorts
25	Deposit D2 SiO_2	Unaxis PECVD	10 μm SiO_2 using recipe in Table 5
26	Measure oxide thickness	Nano-spec Refractometer	
27	CMP on SiO_2	Logitech PM5 Polisher	120 m at 70 rpm
28	Check oxide surface	KLA-Tencor P15	Step profile and clean with HF(1%)
29	Deposit D2 SiO_2	Unaxis PECVD	10 μm SiO_2 using recipe in Table 5
30	Measure oxide thickness	Nano-spec Refractometer	
31	Deposit ”Via mask” metal Al(Si)/Al(Cu)	Unifilm Sputterer	1. Deposit Ti 600 Å- See Table 5 2. Deposit Al(Si) or Al(Cu) 1 μm - See Table 5
32	Litho ”Via mask” metal	MA-6 Mask Aligner	See Table 9
33	Etch ”Via mask” metal	Plasma Therm ICP	1. Wet etch for 15 m - See Table 8

Continued on Next Page...

Table 10 – Continued

Step	Process Step Name	Equipment	Recipe
			2. Dry metal etch - See Table 6
34	Etch Via SiO_2	Plasma Therm ICP	Etch SiO_2 ~ 20 μm - See Table 6
35	Strip photo-resist	Vision RIE	1. Rinse with acetone 2. Sonicate in acetone for 2 m 3. Rinse with IPA 4. O_2 plasma descum for 10 m
36	Clean Via contact metal	Vision RIE	Ar plasma descum for 5 m
37	Deposit M4 metal (AlSI/Al(Cu))	Unifilm Sputterer	1. Deposit Ti 600 Å- See Table 5 2. Deposit Al(Si) or Al(Cu) 1 μm - See Table 5
38	Measure sheet resistance	Signatrone 4-point probe	
39	Litho M4	MA-6 Mask Aligner	See Table 9
40	Etch M4	Plasma Therm ICP	1. Wet etch for 15 m - See Table 8 2. Dry metal etch - See Table 6
41	Strip photo-resist	Vision RIE	1. Rinse with acetone 2. Sonicate in acetone for 2 m 3. Rinse with IPA 4. O_2 plasma descum for 10 m
42	Measure metal thickness	KLA-Tencor P15	Metal step height
43	Electrical test	Probe Station	Probe test wirebonding pads to test for shorts
44	Etch SiO_2	Plasma Therm ICP	Etch SiO_2 ~ 2 μm - See Table 6
45	Resist protection coat	Spinner	Protect wafer front with Shipley 1827 PR
46	Mount Wafer on carrier		Use Cool Grease to attach wafer to carrier (front side down) and shadowmask
47	Deep Si etch	Plasma Therm ICP	Etc Si 100 μm using recipe in Table 7
48	Back-side M1 etch	Plasma Therm ICP	1. Wet etch for 6 m - See Table 8 2. Dry metal etch of 0.3 μm for 6 m - See Table 6
49	Strip photo-resist	Vision RIE	1. Rinse with acetone 2. Sonicate in acetone for 2 m

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Table 10 – Continued

Step	Process Step Name	Equipment	Recipe
			3. Rinse with IPA 4. O_2 plasma descum for 10 m
50	Back-side SiO_2 etch	Plasma Therm ICP	Etch SiO_2 ~ 3-6 μm - See Table 6
51	Si etch pullback	Plasma Therm ICP	Etc Si ~ 20 μm using recipe in Table 7
52	Clean back-side contacts	Vision RIE	O_2 Descum
53	Deposit Backside Ti/Au	CVC Ebeam Evaporator	Ti 1Å/s and Au 1.5Å/s
54	Dice	Dicing Technologies Saw	

The following process flow describes the fabrication sequence of the structure shown in Figure 23. Since the traps of generation **A** and **B** have same cross-section and build-up, the same set of processes is used for the fabrication of both generations of traps. Generation **A** trap use Al(Si) as a conductor material and generation **B** traps used Al(Cu) material. Since the process recipes for depositing and etching Al(Si) and Al(Cu) are similar, the process flow remains same. There are some other differences between generation **A** and **B** traps that are discussed in Section 6.4.

1. To begin, a double-sided polished wafer of thickness $\sim 480\,\mu$m is cleaned using standard RCA cleaning procedure used in the CMOS fabrication industry. The cleaning procedure removes organic and ionic contaminants and strips native oxide. The RCA cleaning procedure is a five-step process:

   (a) The wafer is soaked in Piranha for 10 minutes, while Piranha is heated at the temperature of 120°C. The Piranha is a mixture of sulfuric acid and hydrogen per oxide with the composition of 3:1::H_2SO_4:H_2O_2. The Piranha mixture removes organic and ionic contaminants.

   (b) Rinse with running de-ionized (DI) water for five minutes.

   (c) Soak in Buffered oxide Etch (BOE) solution for 10 seconds to remove the native oxide.

   (d) Rinse with running DI water again to remove any BOE solution residue.

   (e) It is recommended to spin-dry the wafer to get rid of any water marks and residue caused by contaminants from water. We use a spin-dryer, that spins the wafer at 100 rpm for 3 minutes.

2. The first mask layer is for the back-side angled etching of the slot. This etching is anisotropic wet etching and is performed using potassium hydroxide (KOH) solution. A silicon nitride (SiN) mask is used for the KOH-etch. A 6000 Å thick SiN film

is thermally deposited on both sides of the wafer using a LPCVD Trystar Nitride furnace. The process recipe of the SiN deposition is given in Table 5. It is a low-pressure (130 mTorr), low-stress and slow deposition process with a rate of 40 – 50Å/s .

3. Photolithography is performed to pattern the SiN. For photolithography of SiN, the **Litho SiN** recipe is used (see Table 9). Photo-resist is patterned on the back side of the wafer. The corresponding mask is shown in Figure 30. The mask dimensions are chosen in such a way that the KOH etch stops itseld along the ⟨110⟩ crystal plane.

4. Once the photo-resist is patterned, the SiN is etched using the dry-etch RIE recipe given in Table 6. Since the nitride-etch process is Flourine-based process, it roughens the Si when it is exposed to the plasma. Care must be taken not to over-run the etching process. This is done by exactly measuring the SiN using refractometry.

5. After the SiN is patterned, the photo-resist is stripped away. Stripping of photo-resist is achieved by rinsing in acetone, sonicating in acetone for two minutes, rinsing with IPA, and finally using dry RIE oxygen plasma etch (also know as descum). The process recipe and parameters for the O_2 plasma descum process are given in Table 6.

6. Once the SiN is patterned and the wafer is cleaned, a KOH anisotropic etch is performed by soaking wafer in the KOH solution for several hours. The recipe for this step is given in Table 8. The wafer has a ⟨110⟩ crystal plane exposed. The KOH etches significantly faster along ⟨111⟩ crystal face, and it self-limits when the two ⟨111⟩ planes meet from both sides of etching through a rectangular slot. An angled slot approximately 400 μm deep is etched away in this step using the 570 μm wide slot patterned in step 1.

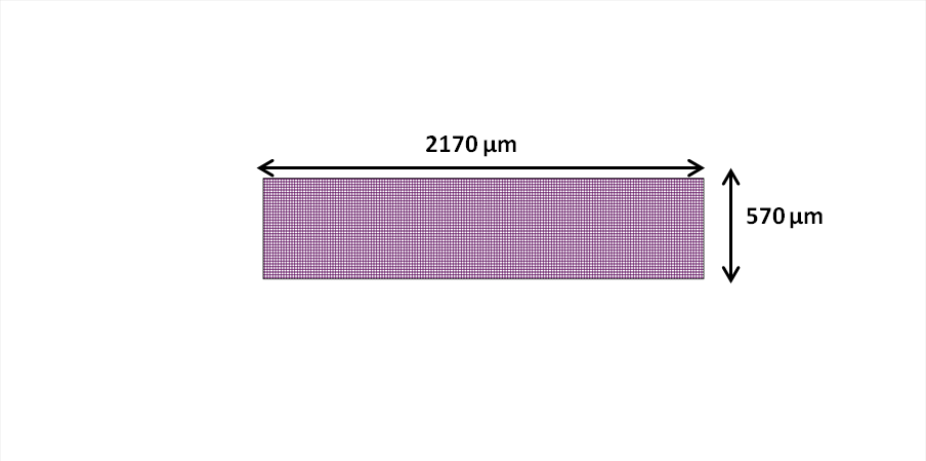

Figure 30: KOH solution etches away the Si from the rectangle shown in this mask along $\langle 111 \rangle$ face.

7. After the KOH slot is etched in the Si, the SiN mask has to be removed. It is removed by soaking the wafer in 49 % hydro flouric acid (HF) solution. HF etches away the SiN in ~ 3 hours (6000Å) from both sides of the wafer. At this stage, the back side of the wafer is shown schematically in Figure 31. A 3D drawing of the slot is shown in Figure 31(a). A micrograph of the back-side KOH-etched slot cross-section is shown in Figure 31(b).

8. After stripping the SiN mask layer, the wafer is wet-cleaned again using the BOE solution. After soaking the wafer in BOE for 10 seconds, it is rinsed with running DI water for five minutes and then spin dried.

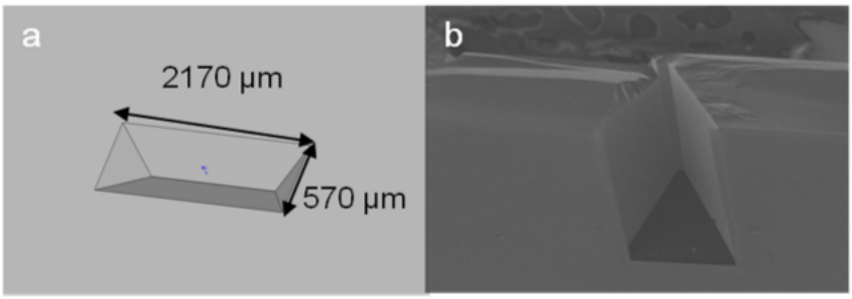

Figure 31: Schematic and SEM image of KOH-etched slot on the back side.

9. At this stage, the wafer is ready for front-side processing and the trap structure build-up. The first step is to deposit the M1 metal layer. For generation **A** traps Al(Si)

was deposited and for generation **B** Al(Cu) was deposited. Deposition recipes for both compositions are same and given in Table 5. The interfacial layer for adhesion is deposited first as ~ 600 Å of Ti. Next a 3000 Å Al is deposited with a Unifilm Sputterer tool. The deposition conditions are listed in Table 5.

10. This M1 metal layer is patterned using a second mask layer, which is laid out in Figure 32. Patterning of this metal layer is performed through the **Litho M1** recipe given in Table 9. This layer requires back-side mask alignment. Since the front-side slot needs to be aligned to the back side, back-side-alignment markers have to be used. The alignment marks for all the layers are shown in Figure 42 and the schematic of this step is shown in Figure 43(b). After developing the photo-resist, Al and Ti are etched using wet-etch recipes. The Si under the M1 layer has to be kept smooth. It was observed during process development that using a dry-etch process at this stage causes the Si surface to be roughened from ion bombardment in RIE/ICP process. Roughening of the Si surface causes extra topographical features subsequently deposited layers that result in hard-to-etch areas. Al is etched by soaking in Al-etchant type A for 15 minutes and Ti is removed by soaking the wafer in ethylene glycol buffered oxide etch (EGBOE) for two minutes. After patterning the M1 layer, the photo-resist is cleaned with acetone-IPA-descum process recipe shown in Step 14 of the Table 6.3. The thickness of the patterned metal is confirmed by measuring the step-height of the profile of the M1 pattern using a profilometer. The sheet resistance is measured using four-point probe. The sheet resistance is usually a good indicator of any residue left-over from the photolithography or etching. Any dielectric contamination on the metal surface will cause the four-point probe to show irregularities in the sheet resistance measurement across the surface. A microscope image of the patterned M1 is shown in Figure 33

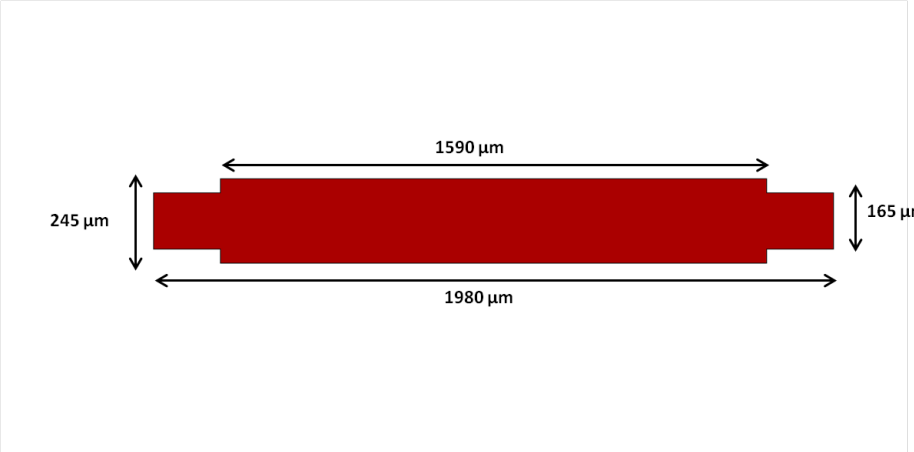

Figure 32: Mask layout of M1 layer. This mask is aligned to the back-side-etched slot. Metal is going to be etched away from the red area. The dimensions of the slots are laid out to allow back-side alignment tolerances.

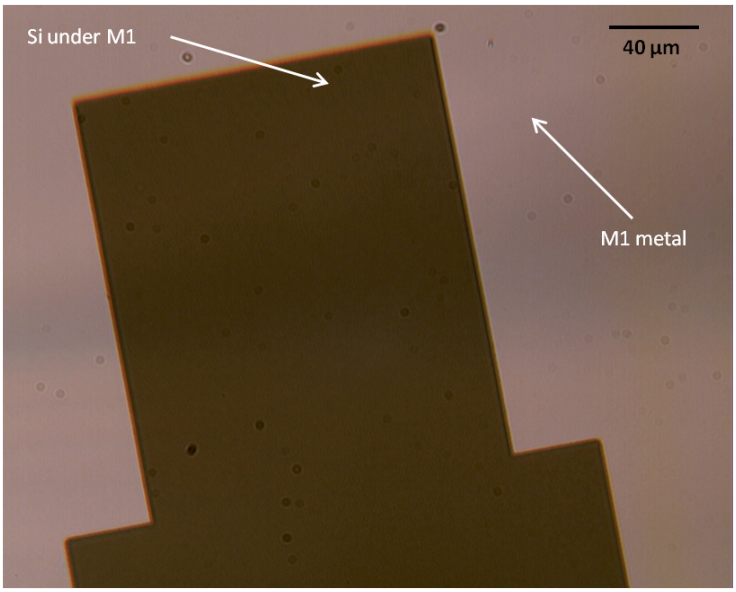

Figure 33: Microscope image of patterned M1. Exposed Si and metal of M1 are labeled.

11. The first dielectric (D1) layer of 1 μm SiO_2 is deposited using the Unaxis PECVD tool. The oxide deposition is conformal and deposited at a high temperature of 250°C. The process recipe parameters are given in Table 5. The Unaxis PECVD equipment does not have loading chamber (loadlock). Extra care is required to ensure of the cleanliness of the process chamber. To assure the repeatability of the process, a one hour high-pressure plasma clean and a one-hour low-pressure plasma

clean are run before oxide deposition in the chamber. As an extra caution, the chamber inside and the O-ring, where the particles are trapped, are wiped off with IPA. Before actual deposition process was started in this chamber, we determined a best known method (BKM) for this tool as follow:

(a) one-hour low-pressure plasma clean,

(b) one-hour high-pressure plasma clean,

(c) open the chamber and wipe-off chamber inside and O-ring with IPA,

(d) run oxide deposition process for five minutes without loading the sample in the chamber. (This is done to pre-coat the chamber,)

(e) load the sample and process for the desired time

This oxide deposition process deposits 1 μm in 18 minutes. Afterward the oxide deposition thickness is measured using refractometry. The refractometer measures the exact refractive index of the film on a given substrate. Using its calibration data it determines the thickness of the deposited material.

12. The next step is to deposit the M2 layer consisting of 600 Å Ti and 1 μm Al. Ti and Al are deposited using the Unifilm Sputterer with the deposition conditions given in Table 5. The thickness is verified by measuring the sheet resistance on the Signatrone four-point probe.

13. The M2 is patterned using lithographic recipe **Litho M2** as listed in Table 9. After patterning the photo-resist, the Al and Ti films are etched using the wet-etch recipes given in Table 8 by soaking the sample in Al etchant type A for 15 minutes followed by ICP dry-etch process given in Tables 6 and 8. The M2 layer consists of all the lower DC electrodes and the via-pads for upper DC electrodes. These features are labeled in Figure 43(d) and in the mask layout shown in Figure 34. The M2 mask also patterns the wires for the lower and upper DC electrodes and on-chip capacitors.

After etching the M2 pattern, the photo-resist is cleaned with the standard acetone-IPA-O_2 plasma descum processes. A microscope image of the patterned M2 features on a sample is shown in Figure 35. The main difference between the generation **A** and **B** traps lies in this step. The details of the improvements made in generation **B** traps are given in next section.

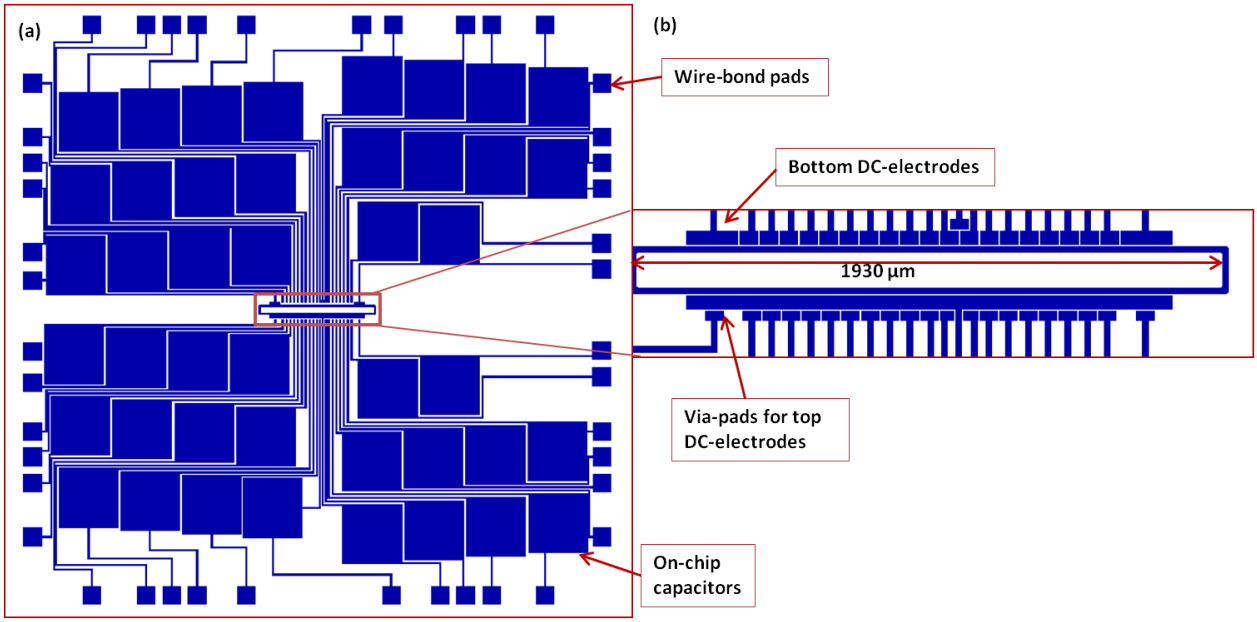

Figure 34: Mask layout of the second metal (M2) layer. (a) the layout of mask of M2 layer and (b) the slot area including bottom DC electrodes and via-pads for top DC electrodes.

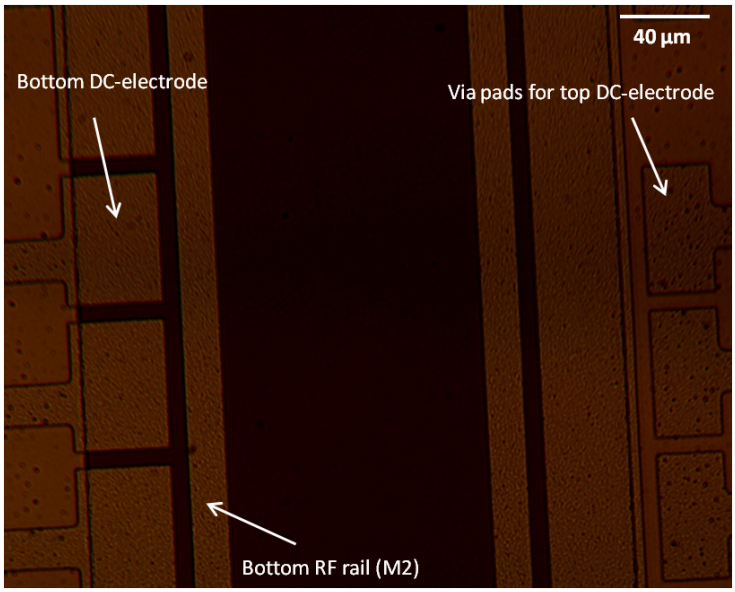

Figure 35: Microscope image of patterned M2 layer. M2 layer contains RF rails, bottom DC-electrodes and via-pads for top DC-electrodes.

14. After the M2 is patterned, metrology is performed on the etched metal layer. The sheet resistance is measured using four-point probes, the step height is measured using a profilometer, and regressive electrical testing is conducted using electrical probes. In this electrical testing, continuity between the DC electrodes and the corresponding wire-bond pads as well as the isolation of each wire-bond pad from its neighbors is verified. These electrical tests are crucial because vertical build-up of the structure will make it impossible to correct any lithographic errors that are detrimental to the device at the later stage. At this stage, the critical defects can be corrected by repeating the photolithorgaphy and patterning processes.

15. Once the M2 layer is patterned and verified electrically, a 10 μm of SiO_2 D2 layer is deposited. The total thickness of D2 layer is 20 μm , achieved by depositing of 10 μm each. Each 10 μm SiO_2 layer is deposited in 2 μm steps. Breaking the deposition in 2 μm steps helps in maintain the stress of the wafer within critical limits (< 10 MPa). The larger stress can increase the adhesion problems of the metal surfaces deposited above and under the oxide layers. Additionally, 2 μm SiO_2 layers maintain control of the particle contaminants. After each 2 μm layer, the BKM of the SiO_2 deposition as given in Step 11 is performed and next layer is deposited. The schematic of the sample build-up is shown in Figure 43(e).

16. Before the next 10 μm SiO_2 is deposited, the thick film of SiO_2 deposited in last step has to be smoothened. At this stage, chemical mechanical polishing (CMP) is performed. CMP takes away 3 μm of the SiO_2 and smooths the profile of the oxide around the active region of the structure. The oxide profile over the gaps between the DC electrodes have approximately one μm step before CMP. The CMP polishes the oxide so achieve 2000 Åstep over these gaps. The main reason for this polishing is to get rid of the topography and the steps caused by previously deposited layers. Removing these surface steps makes subsequent etching easier and cleaner. The

CMP process takes approximately 3 hours.

17. The CMP process leaves some residue from the slurry chemical used for the CMP process. This residue sticks to the surface and can be removed by soaking the sample in 1 % HF solution for 40 seconds. The HF solution etches some SiO_2 away. However, due to its weak concentration, the etch rate is sufficiently slow $\sim$ 1000Å/m , that only less than 1000 Åis removed. Since the wafers have KOH-etched slots with a remaining 80 μm of Si in them, the wafers are fragile and high-power sonication is avoided. The residue remaining from CMP is not optically visible even under Nomarsky microscopy. Therefore, the sample is inspected under atomic force microscope (AFM) for any features that are near the size of the colloidal slurry used for CMP. The slurry used for CMP is a 0.6 μm colloidal Silica slurry. Any features near $\sim$0.5 μm are indicator of residual particles from the CMP process. If a significant amount of these particles are found after the first cleaning, another quick HF(1%) is performed. After cleaning up the residue, another 10 μm of SiO_2 is deposited. Since approximately 2-3 μm of SiO_2 was removed in previous CMP step, after the second 10 μm of deposition, the final SiO_2 D2 layer thickness is $\sim$17-18 μm .

18. After completing the thick SiO_2 D2 layer, 600 Å Ti and 1 μm Al metals are deposited as the third metal "Via-mask" layer. This layer acts as a mask for the oxide-etch in the following step. The sheet resistance is verified after the deposition.

19. The via-mask layer is patterned so that the vias for top DC electrodes can be connected to the via-pads patterned on M2 layer. In the same mask the vias for the wire-bond pads are also patterned. The mask used in this step is shown in Figure 36. The photolithographic recipe used for this layer is the **Litho "via-mask" metal** as given in Table 9. After the photo-resist is baked and the pattern is developed, the metal deposition is performed in two steps. The etchant type A is used to etch Al and the sample is soaked in etchant for 15 minutes. This is followed by an ICP dry etch

with the recipe given in Table 6. After etching the metal, the photo-resist is cleaned with the acetone-IPA-O_2 plasma descum processes. An optical microscope image of the patterned via-mask layer is shown in Figure 37.

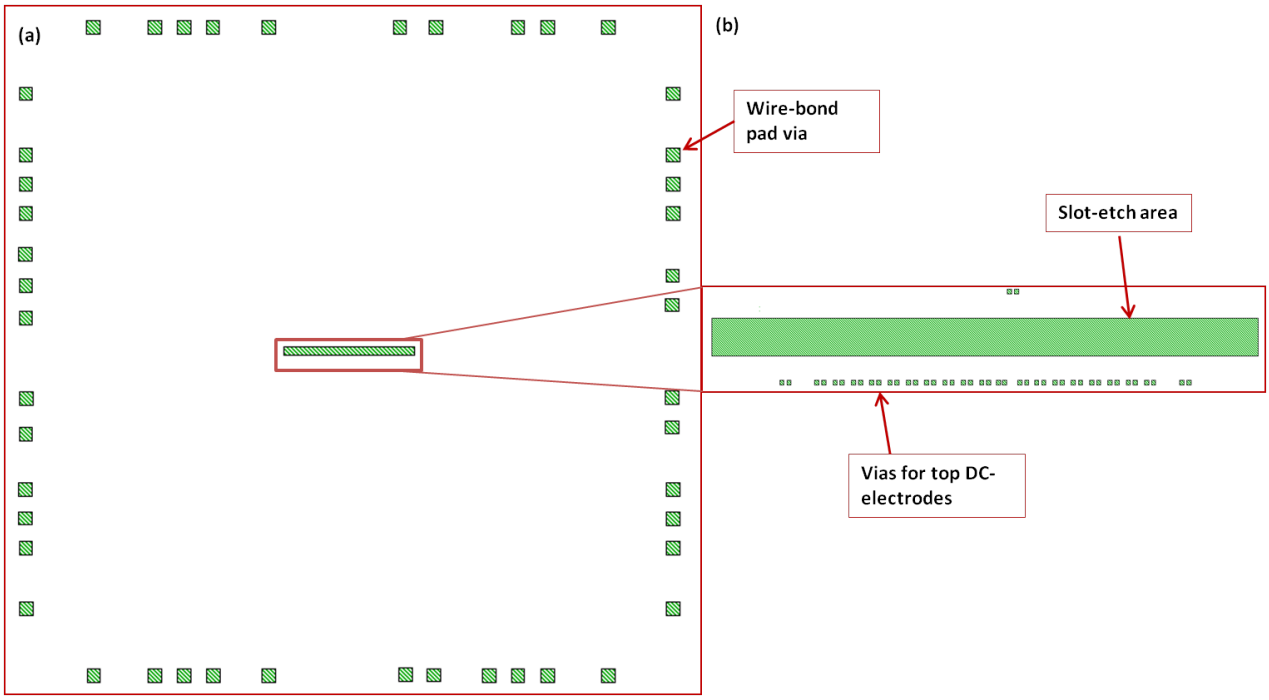

Figure 36: Mask layout of via-mask layer. (a) the die-level via-mask and (b) shows the vias around the slot and via pads on M2.

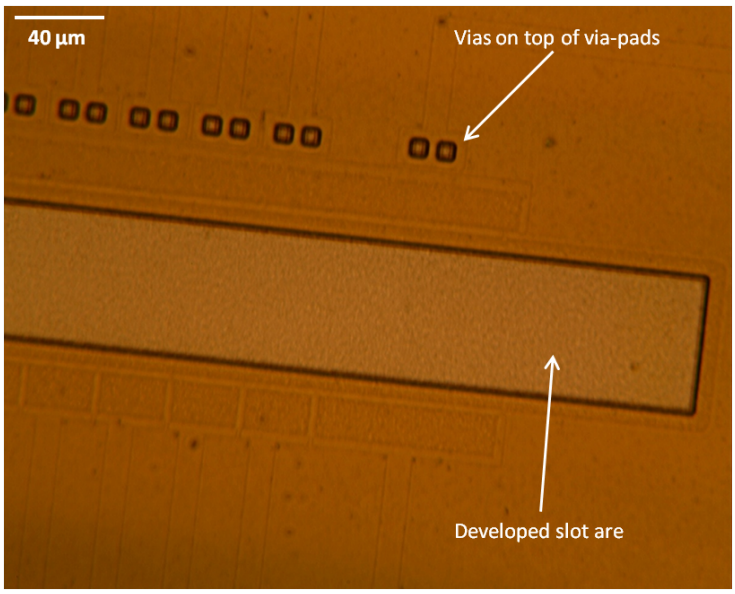

Figure 37: Microscope image of patterned metal via-mask layer. The image shown here has vias and the slot areas developed after photolithography.

20. With the via-mask patterned in the metal, the deposited oxide D2 layer is exposed in the areas where vias are opened. The oxide is etched using the ICP. Etching of this oxide is performed in 2 μm steps. Additional wet-etching is done by soaking wafer into EGBOE to supplement the dry etching. This wet-etch process removes any residual oxide left during the ICP etching and cleans other impurities from the oxide layer, that in some cases, stop the dry etching process. Typically, the wafer goes through several microns of over-etching process due to the differences in etch rates for different parts of the chip. In the slot area, the oxide is deposited on the roughened Si substrate, while in the wire-bond pad areas the oxide is on top of the smooth metal surface. This roughened profile of deposited oxide makes the slot area oxide harder to etch and as a result it requires significant over-etching ($\sim$ 50%). A schematic drawing of this step is shown in Figure 43(g) and a microscope image of the sample after it has gone through 6 μm of oxide-etch is shown in Figure 38.

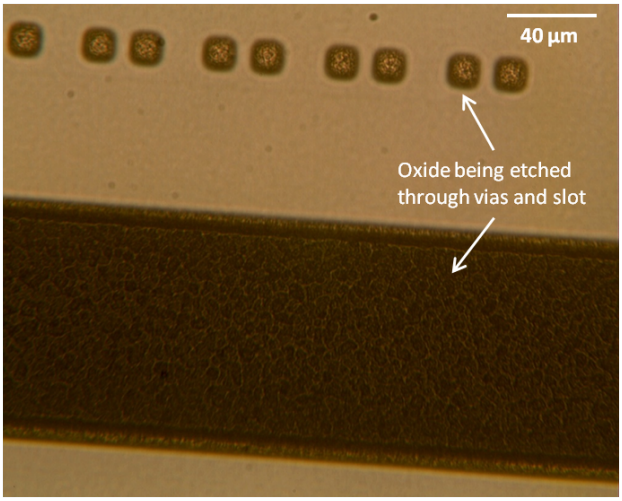

Figure 38: Microscope image of the sample while it has gone through 6 μm of oxide-etch.

21. Once the oxide is etched away from the slot area and the bond-pad vias are exposed, the metal is cleaned by an Argon (Ar) plasma descum and a new metal (M4) layer of 600 Å Ti and 1 μm Al is deposited. The recipe for Ar plasma descum is given in Table 6. Ar plasma descum cleans the native oxide built-up on the Al and the residue from the oxide-eth process.

22. The M4 layer is patterned with the mask shown in Figure 40. The photolithographic recipe **Litho M4** for this step is different from the other etched-metal layers. The difference is due to the presence of $\sim 20\ \mu$m vias that cause the photo-resist to settle down into the vias during baking of the photo-resist. As a result, the photo-resist spinning speed and the UV-exposure time are modified. This recipe is given in Table 9. A schematic for this step is shown in Figure 43(i). The metal is etched in this step using a combination of wet and dry-etch recipes given in the Table 6. The photo-resist is cleaned-up using the acetone-IPA-O_2 plasma descum processes. The M4 layer metal sheet resistance is measured. Since the M4 layer forms the top DC-electrodes, electrical connections are verified by probing the DC-electrodes and corresponding wire-bond pads. Contact resistances are measured and expected to be within $\sim 10\ \Omega$ range. The contact resistances for the generation **A** traps were found to be in $\sim 100\ \Omega$, a value large enough to be problematic as will be discussed in next chapter. A microscope image of the patterned M4 layer is shown in Figure 39.

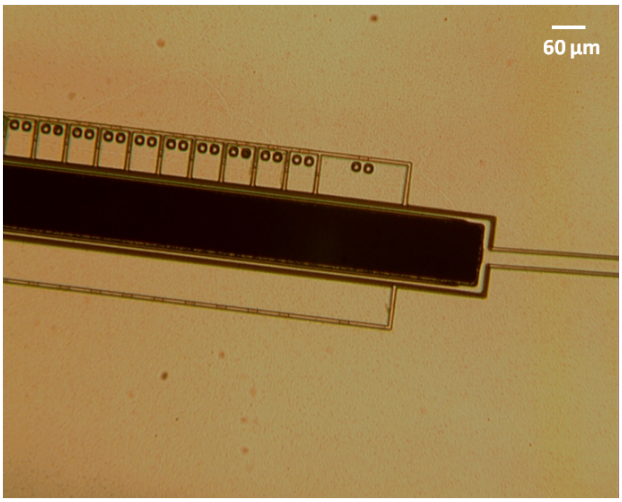

Figure 39: Microscope image of the top layer (M4) pattern of generation A trap.

23. After the M4 layer is patterned with top DC-electrodes, RF-rails, and wire-bond pads, SiO_2 is exposed in the gaps between electrodes. As a precaution, 2 μm of SiO_2 is etched away in the gaps using RIE process. This is done to avoid any contaminant particles that could cause an intermittent short. This etch is done using the dry etch

recipe given in Table 6.

24. At this point, the wafer's front-side processing is complete. The front-side of the wafer is coated with thick photo-resist for protection so that it can be flipped for the back-side processing. The first step on the back-side is Si etching. To etch the Si, the flipped wafer is mounted on a carrier wafer. This is done as a precaution so that if actual sample is etched-through, the plasma inside the chamber will not cause any damage to the chuck of the chamber. The wafer is mounted on the carrier and the shadow-mask on the wafer using cool-grease.

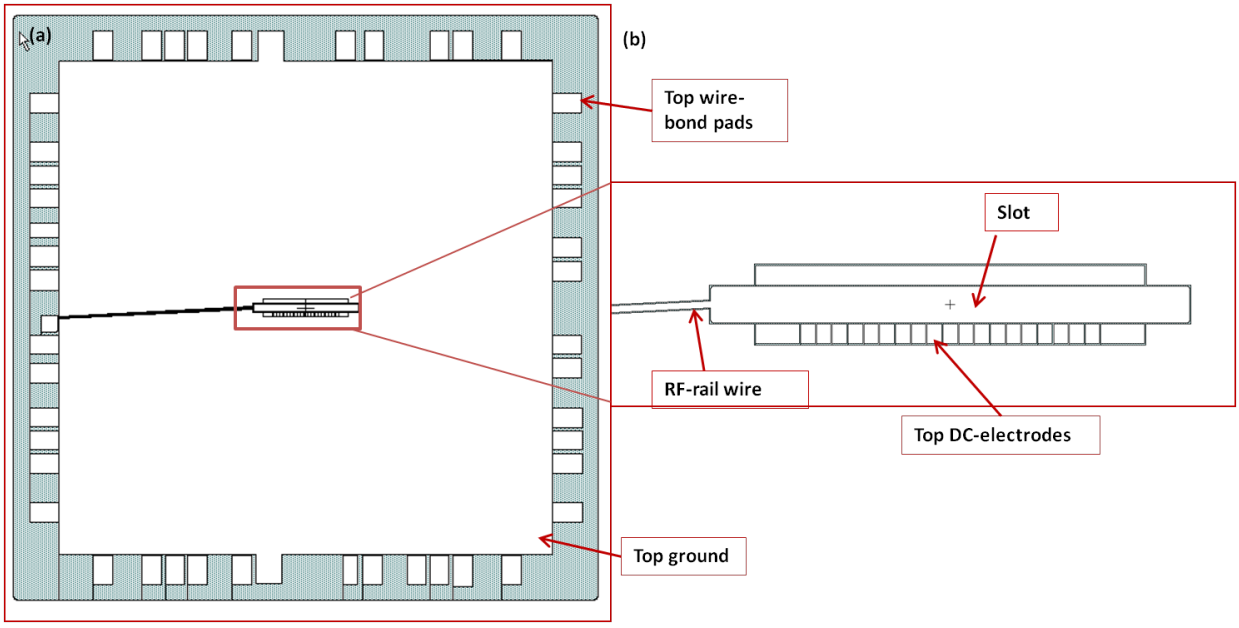

Figure 40: Mask layout of top-DC-electrode metal (M4) layer. (a) the die level mask layout of M4 and (b) the areas which will be patterned in reference to M2 and M3 layers. White spaces in (b) are shown with arrows representing top DC-electrodes.

25. From the back side of the wafer, the remaining Si in the KOH-slots is etched away so that metal deposited from the top is exposed. For the generation **A** traps, this top metal is deposited during M4 layer deposition. For the generation **B** traps, the metal exposed from the back-side is M1 with M4 deposited on top of it. The Si-etch recipe is given in Table 7. It is the Bosch process and consists of three steps in a cycle. The first deposition step deposits CF_4, to coat the sidewalls to make this process isotropic.

The second and third etch steps are fluorine-based processes to etch Si. In this overall step approximately 100 μm of Si is etched with 0.65 μm /m etch rate. Once the entire slot area is exposed from the back side, M4 and M1 is etched from the back side using the metal etch recipe given in Tables 6 and 8. As a result, the through-wafer slot completely opens up, except that it is now coated with the resist on the front side as shown in Figure 41.

26. At this time the photo-resist, which is exposed from the back-side of the slot, is removed. In the **A** generation of the traps, this was not removed resulting in a thin insulating layer near the RF rail. This thin layer was formed due to the photo-resist being exposed to the plasma in RIE metal etch process and the following by oxide-etch. For **B** generation traps, the photo-resist is removed as soon as the slot is open from the back-side and cleaned with the standard processes of acetone-IPA-O_2 plasma descum.

27. After the metal is removed from the back-side, approximately 3-6 μm SiO_2 is etched. This SiO_2 is exposed after metal M1- or M4-etch is etched away. A micrograph of the SiO_2 on top of the M2 layer viewed from back-side is shown in Figure 41. Only 1 μm of this oxide is from the D1 deposition layer. The remainder of the SiO_2 is over-etched to recess some oxide in the gaps between electrodes. Since the atomic flux is going to pass through the slot, entering from the back-side of the trap, it is very important to recess the oxide between the electrode gaps to avoid any shorting caused by the atomic flux. The oxide is etched using dry etch recipe shown in Table 6.

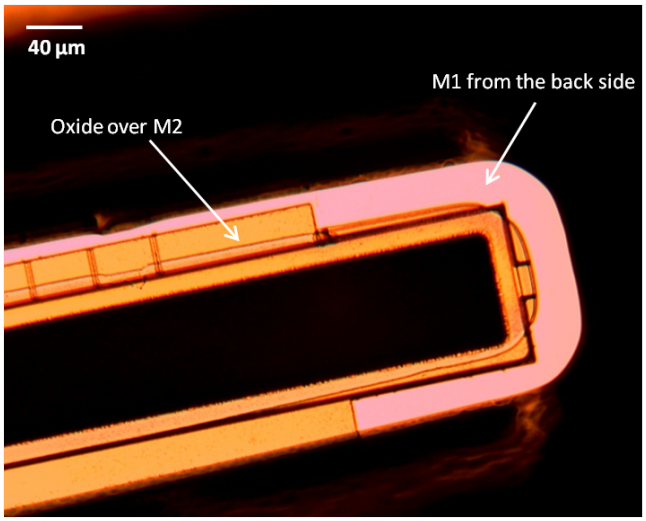

Figure 41: Microscope image of back-side of the sample of generatin A trap. Si is pulled back all the way so that M1 slot is exposed from the back-side. At this stage oxide is exposed and has to be removed by dry etch.

28. More Si is etched using the recipe in Table 7 until the DC electrodes are exposed. This etching also exposes the edge of the M1 slot formed in first step. After the complete slot has opened, the exposed metal is cleaned using the O_2 plasma descum. This gets rid of any residue left over from the photo-resist or multiple etching processes.

29. This ends the structure build-up. Ti/Au layers are now deposited on the back-side to protect the slot areas. The back-side chip surface has to be Au-coated to be soldered on the carrier. Ti is used as an adhesion layer between Si and Au. The Ti and Au in this step are evaporated using an E-beam evaporator. The recipes are given in Table 6.3.

SEM images of the fabricated generation **A** trap are shown in Figure 44. The top view of the trapping region of the trap is shown in Figure 44(a), the back-side view is shown in Figure 44(b), and the cross-section SEM images are shown in Figures 44(c) and 44(d).

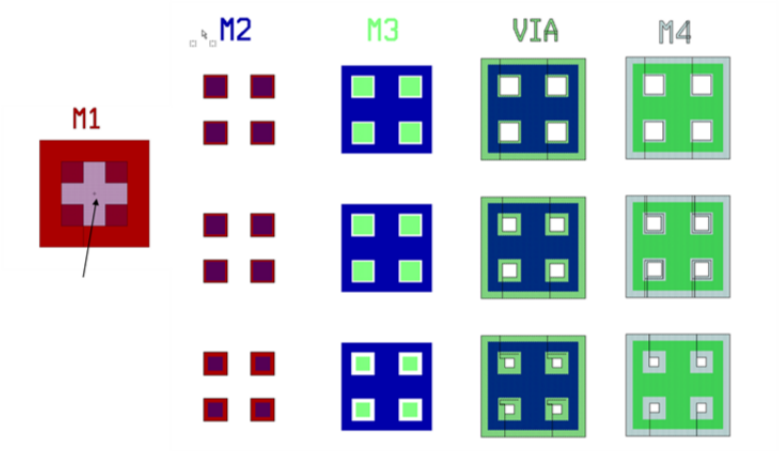

Figure 42: Alignment marks for all the mask layers.

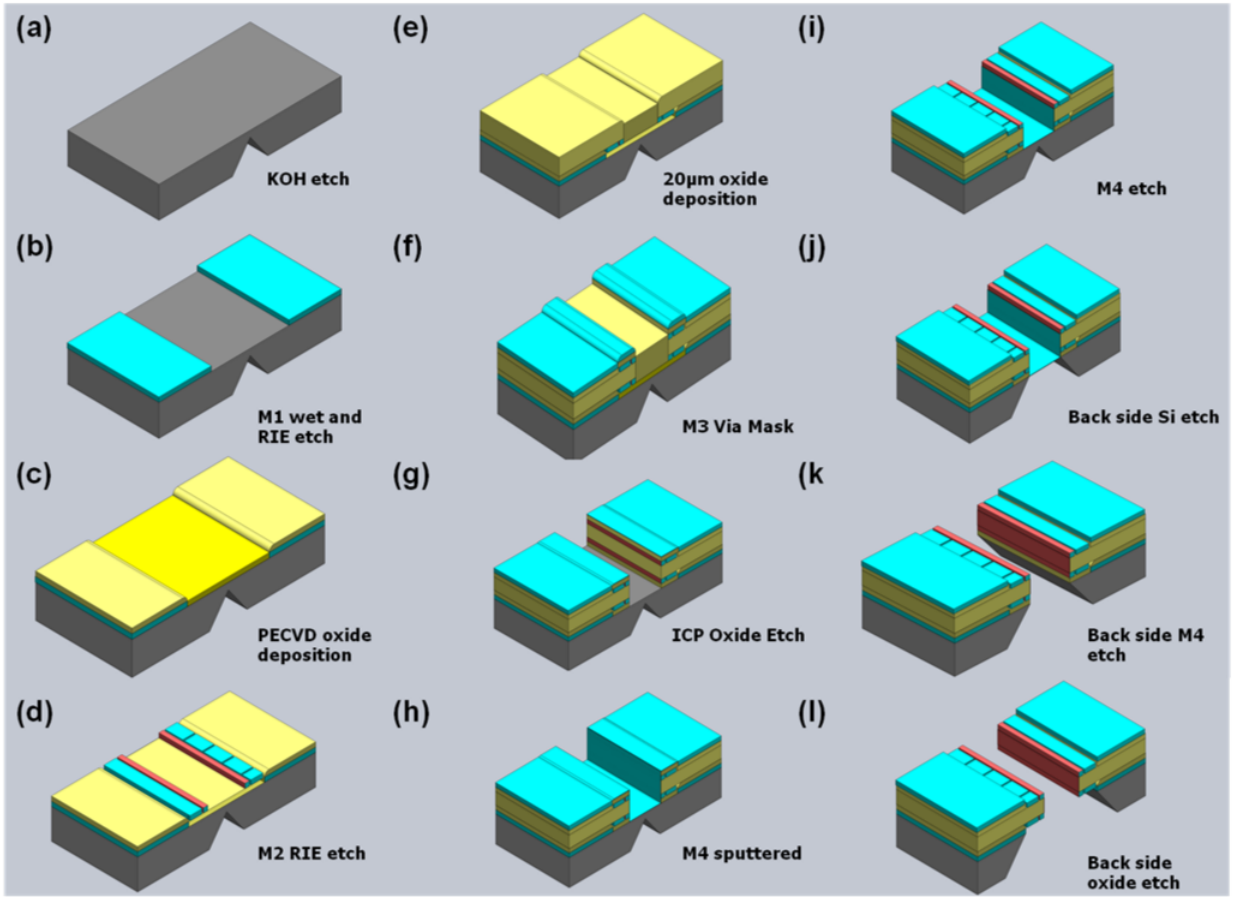

Figure 43: Schematics of the structure build-up as fabrication steps are performed on the Si wafer.

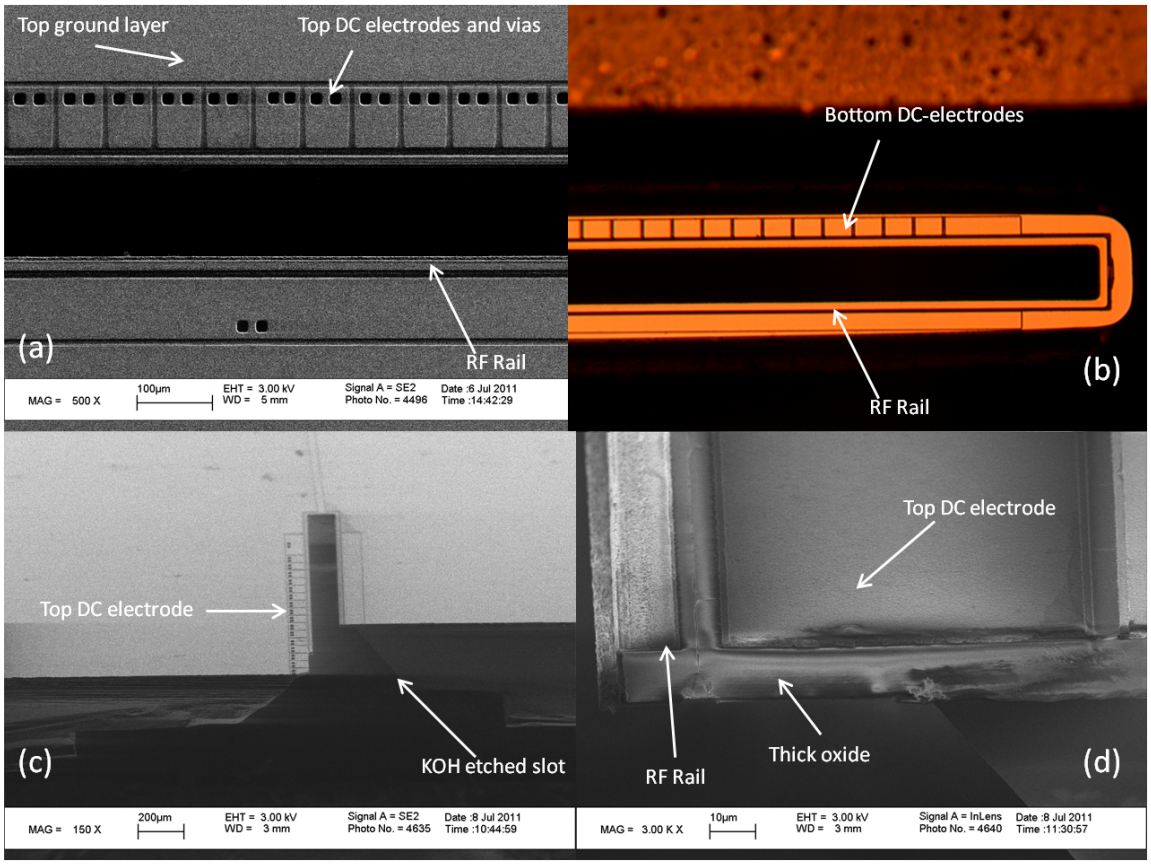

Figure 44: SEM images of the fabricated trap. (a) the top view of the trap slot, DC electrodes, vias, and RF rail and (b) the back-side DC electrodes. (c) and (d) the cross-section of the trap.

6.4 Improved symmetric trap fabrication

During the testing phase, several factors were found that required changes in the mask layouts and fabrication processes. These changes and improvements were incorporated in the generation **B** trap. .

6.4.1 Layout improvements

1. During the initial electrical testing of the generation **A** trap chip, it was found that there was a mask design error, that left the bottom long trap electrode disconnected from its wire-bond pad. Although this 2 μm defect caused the long electrode to remain disconnected from the wire-bond pad in many chips of the wafer, for some

chips the defect was too small to be resolved during contact lithographic process resulting connectivity to the long electrode and testable chips. The chips with disconnected electrodes were not tested since the floating electrode would certainly charge to some unknown uncontrollable voltage. This error is fixed in M2-layer mask of the generation **B** traps.

2. The dry RIE etch process to remove D2 (thick oxide) layer for the generation **A** trap had different etch rates for the bond pad vias and the trap slot area. The etch rate was much faster for the bulk oxide that was being etched in the slot area than the oxide that was exposed in the smaller areas such as vias. To remove the oxide from the vias completely the etch process had to be run long enough to cause the etching of the Si that got exposed after the oxide was removed in the slot area. was under the oxide in the slot area. The processing of Si with the oxide-etch DRIE recipe roughened the Si.Following the oxide-etch process, some oxide residue was left over which could not be etched away with dry or wet etch. This thin layer of residual SiO_2 got mixed with the Al that was being etched from the back-side. And the mixture of Al, SiO_2 , and the photo-resist (coating the front-side of the wafer) formed a thin layer of mixture. This thin layer wrapped around the slot edges when chips were being cleaned. This layer was found to be electrically insulating which could charge up when high voltage is passed through the RF rails of the trap. Although it is a process issue, it can easily be fixed by improving the mask design and changing the process flow. In the original set of masks (for generation **A** as shown in Section 6.3, when the first set of metal is etched, the metal etches away from a larger slot area. The mask is modified to leave the metal in the center of the slot, which can easily be etched away at the end. The modification is to change the rectangle opening to a rectangle of strip. New mask layout of M1 mask is shown in Figure 45. This mask is used to build the generation **B** traps.

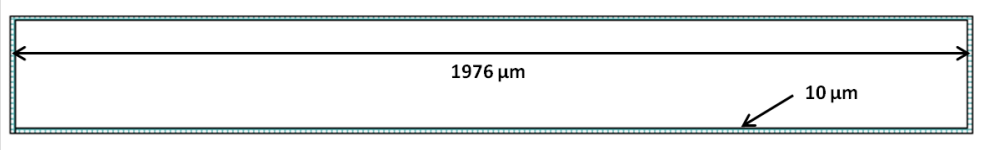

Figure 45: M1 mask layout for the traps of generation B . M1 slot is modified so that metal remains in the slot area, which acts as a mask for deep oxide etch after via-mask pattern.

3. The alignment of the front-side slot to the back-side KOH-etched slot, is prone to errors due to the back-side alignment limitation of the mask aligner equipment available. For the generation **A** traps, this error resulted in significant M1 removal around the trapping region during the back-side metal etching. As a redundancy, for generation **B** traps two new ground electrodes were added in the second metal layer (M2) along with two new bond pads are also added. The modified mask is shown in Figure 47.

4. Four new ground bond pads were added for generation **B** traps, two for the M1 and two for the M4 ground layers, to have redundant pads on each side. This allows flexibility for rotating and installing the chip on the carrier in any orientation since all the sides have two ground pads available.

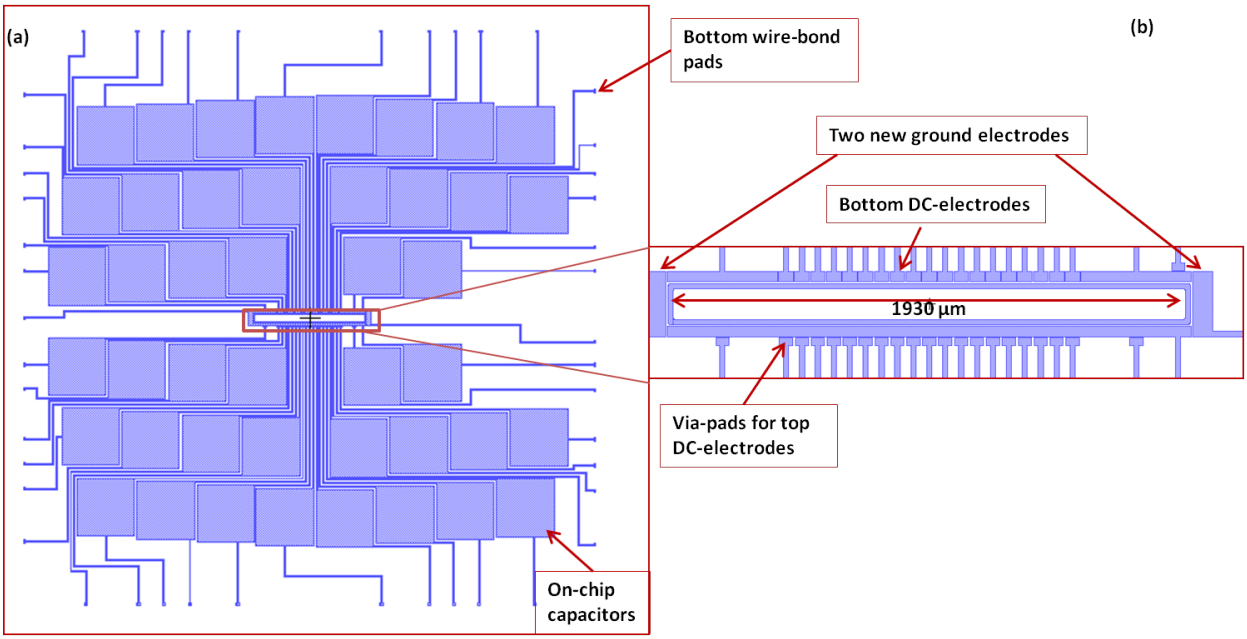

Figure 46: M2 mask layout for the traps of generation B . New ground electrodes, and wire-bond pads are added in the new layout. Wire-bond pads are modified to be big enough to cover the vias from the M4 layer.

5. The upper central electrode was marked with a cross that allows simple and accurate laser alignment for generation **B** traps. Laser alignment marks are part of the last mask, which patterns the M4 and top DC-electrodes. The mask layout is shown in Figure 47.

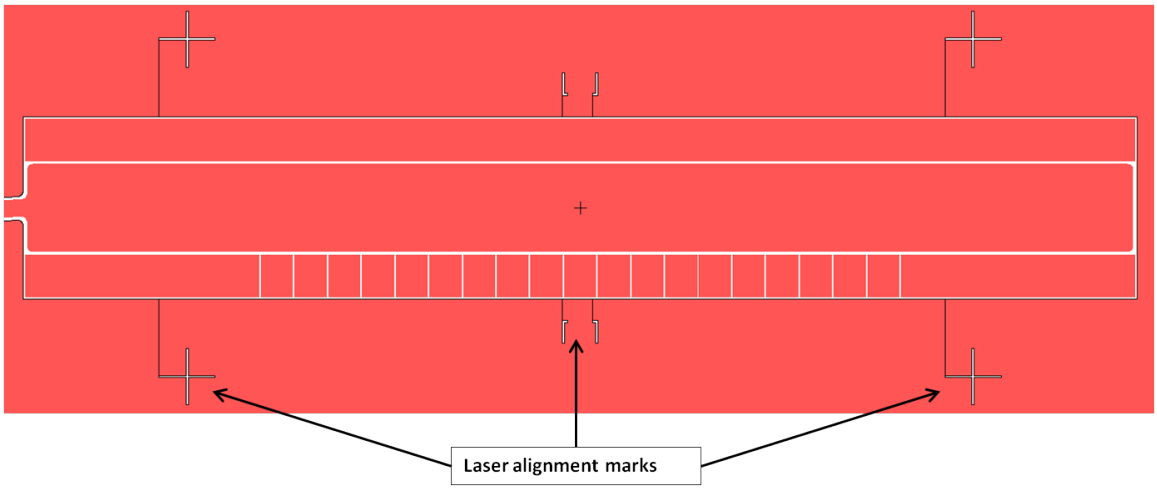

Figure 47: M4 mask layout for the traps of generation B .

6. The large bond-pad vias are reduced in size in generation **B** traps. The main reason

for this change is to make the lithographic process smoother. During the last metal layer (M4) patterning, the photo-resist precipitated down into the large vias used in generation **A** traps. Wire-bond pad vias were changed from 200 μm x 200 μm in generation **A** to 15 μm x 15 μm in generation **B** . With large deep vias, spinning of the photo-resist causes thinning of the photo-resist along the edges of the vias. SEM images of trap **B** on top of M2 wire-bond pads are shown in Figure 48(c). SEM images of the trap **B** are shown in Figure 48.

6.4.2 Process improvements

During the fabrication of the first processing batch, several process issues were discovered and later fixed. When the traps of generation **A** were being processed, a few problems were discovered that were fixed in generation **B** traps. The process improvements incorporated in the generation **B** traps include:

1. During the UHV bake-out at 200°C whisker growth was observed on the trap metal surfaces. It is known that the Al whisker growth is observed at relatively low temperatures (200°C) using the Al(Si) electrode material used in the earlier processing. Higher bake-out temperatures are achieved in the new process using Al(Cu) (1 % Cu impurity) to replace the Al(Si). Etching of Al(Cu) is accomplished using a combination of wet- and dry-etch processes that were developed and are given in the process flow Table 6.3 and etching recipes in Table 6 and Table 8.

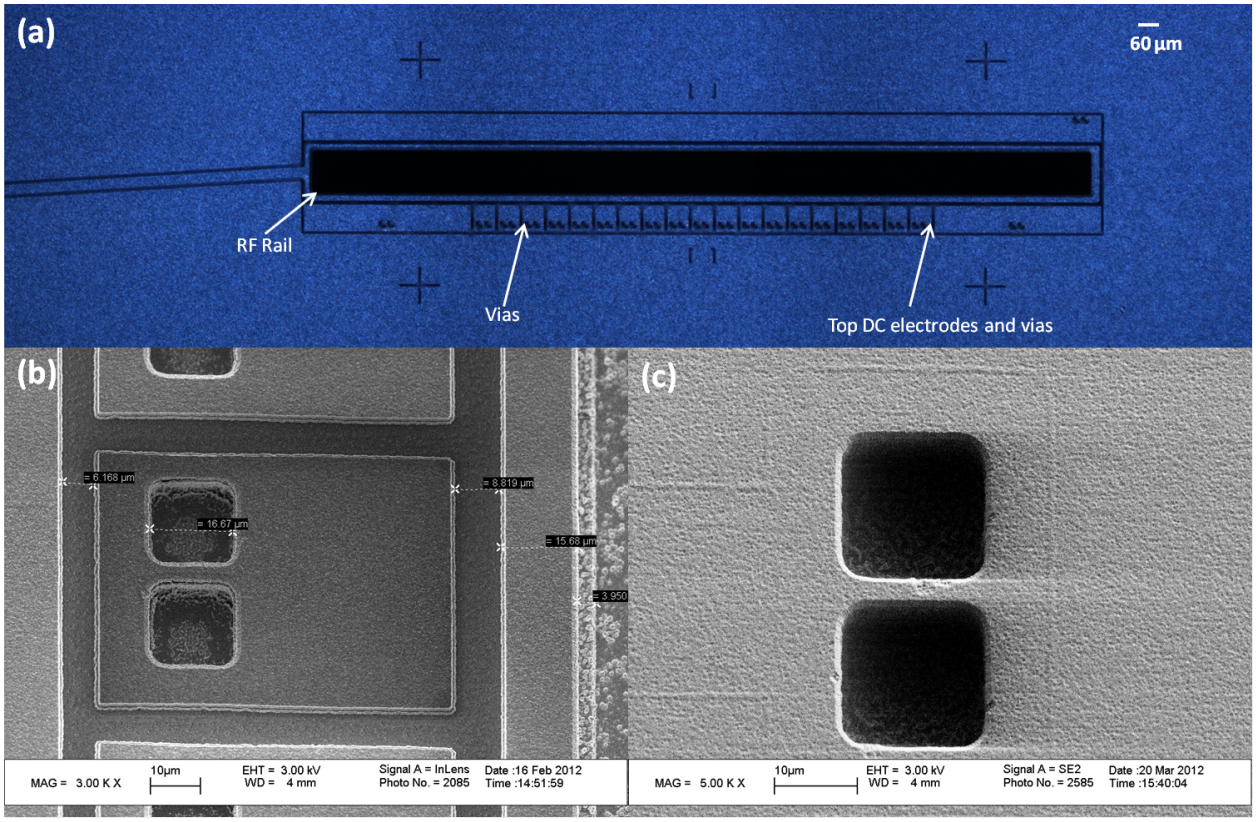

Figure 48: Microscope and SEM micrographs of the second generation (B) symmetric traps. A high resolution microscope image is of the trapping region of the symmetric trap is shown in (a). This trap was tested in May - July 2012 in QIS lab by loading $^{40}Ca^{+}$ ions. SEM image of the top DC-electrode, top RF rail, and vias along with actual dimensions are shown in (b). Wire-bond pad vias being etched as part of revised "Via-mask" are shown in (c).

2. During the generation **A** fabrication, photo-resist stripping relied only on acetone, IPA rinse and dry O_2 plasma etch. During lithographic steps, it was observed that the wafer can be cleaned more thoroughly if it is sonicated in a solvent. Since for the generation **A** traps, the first KOH-etch step of leaves only $\sim$ 80 μm of Si on the KOH slots, the sample becomes too fragile to be sonicated in acetone. For the **B** traps the dimension of the KOH slot was modified so that at least $\sim$ 200 μm of Si was left in the slots. This enabled the photo-resist cleaning recipes as shown in Table 6.3 to include a sonication step. The new KOH-slot mask dimensions are 2321 μm x 470 μm .

CHAPTER 7

EXPERIMENTAL APPARATUS

Ions are trapped in ultra high vacuum (UHV) chambers at the room temperature. The microfabricated traps are packaged on a UHV compatible ceramic pin grid array (CPGA). The CPGA is selected based on the number of DC-electrodes or channels to be controlled. In this chapter the UHV system, experimental setup, laser layout, and collection optics used to test the symmetric traps are described. The symmetric trap packaging, electrical tests and ion trapping results are discussed in Chapter 8. The experimental results of this thesis work include four phases of trap testing. These phases and the traps that were tested are listed in Table 11. The original UHV system was setup in October 2011. It was late modified for each iteration of the experiment based on the type of the trap and the need to optimize the ion-loading. In the following sections all the setups and corresponding modifications are described.

Table 11: Symmetric trap testing experimental phases.

Phase	Period	Tested trap	Loaded
1	Sep 2011 - Jan 2012	Symmetric trap **A**	-
2	Jan 2012 - March 2012	Gen III trap	✓
3	April 2012 - June 2012	Symmetric trap **B** (F6)	✓
4	July 2012 - Nov 2012	Symmetric trap **B** (F4)	✓

7.1 UHV chamber

The main component of the UHV system to trap the ions using microfrabricated ion trap is the chamber. Based on the experience gained in testing surface-electrode traps in GTRI QIS lab, the symmetric trap system used a 6.0" octagonal UHV chamber as shown in Figures 49 and 50. All the components that were acquired from the vacuum system vendors are listed

in Table 12. The chamber consists of the socket assembly that receives the packaged trap on a CPGA, the oven as an atomic source of $^{40}Ca^{+}$, and shields to protect the trap and socket from the oven flux on the back side as well as electrical stray fields on the front side of the trap. Inside the chamber, the socket is wired to four D-type 25-pin connectors so that voltages can be controlled on each DC-electrode of the trap.

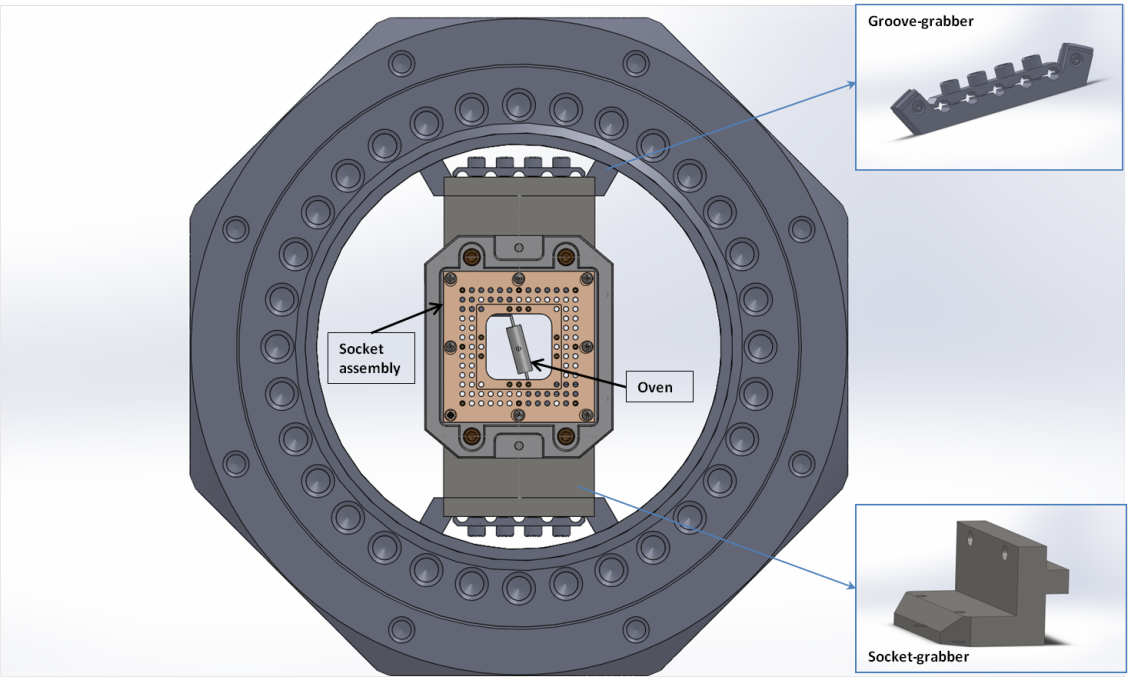

Figure 49: 3D CAD drawings of the front side of the chamber and the parts inside the chamber such as oven, socket assembly, groove-grabber, and socket-grabber.

7.1.1 Socket assembly

Inside the UHV octagon, the trap carrier is mounted on a 100-pin socket. All the components and their materials are chosen to have low vapor pressure so that they are compatible with the UHV requirements of the apparatus. The socket plates were designed to hold PGA10047002 CPGA. They are made of polyether ether ketone (PEEK), which can be operated at temperatures up to 350°C. The exploded 3D-view drawings of the socket plates, socket receptacles, and socket base-plate assembly is shown in Figure 51. These plates were designed in-house and machined at the GTRI machine shop.

The carrier must be pushed hard into its receptacle to ensure good electrical contact.

This requires the socket plates to be firmly attached to the inside of the octagon. Standard parts available at Kimball Physics called ”groove grabbers” were used for firm mounting of the socket assembly to the octagon. The socket assembly is attached with screws to the groove grabbers by in-house machined socket grabbers. These socket grabbers, the socket assembly, and the groove-grabbers are identified in the Figure 49. The base plate, as shown in Figure 51 was designed to hold not only the socket plates of the socket, but also the mounting brackets and the oven mounts on the back side of the base plate as shown in Figure 50. Since the atomic source oven was to be mounted from the back side of the trap chip, the oven mounts were installed on diagonally opposite sides of the carrier opening.

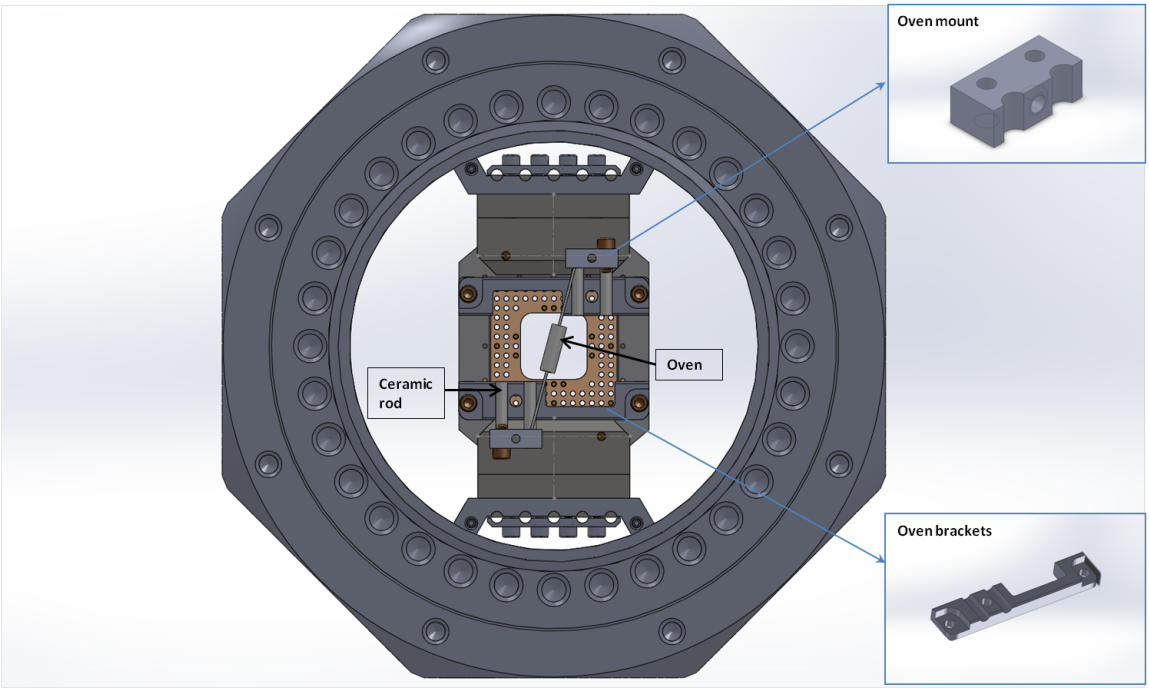

Figure 50: 3D CAD drawings of the back side of the chamber components. Oven, oven mounts, and oven brackets are shown.

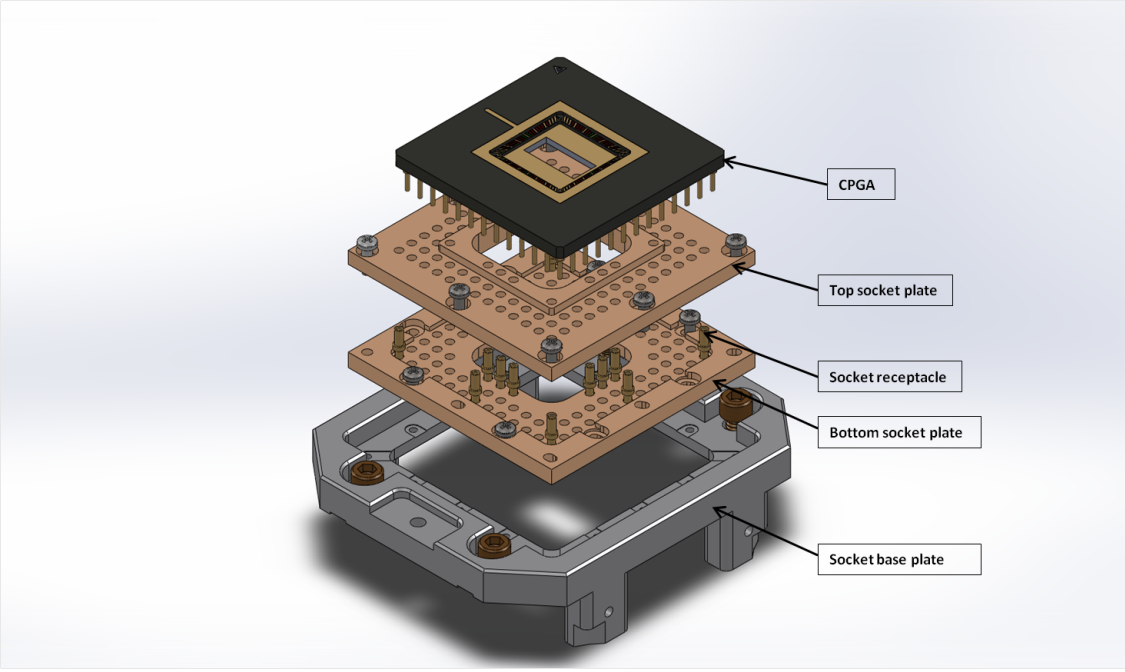

Figure 51: A 3D CAD drawing of the socket assembly and its components in exploded view. Socket plates, receptacles, socket base plate and CPGA are shown. All the parts except receptacles and CPGA are designed in-house.

Table 12: List of chamber components that are acquired from external vendors to build the UHV system for the symmetric trap testing.

Component	Vendor	Part No.
6.0” Spherical Octagon	Kimball Physics	MCF600-SphOct-F2C8
Front-side 6.0” window viewport	Kurt J. Lesker	VPZL-600
Back-side 6.0” window viewport	MDC Vacuum	450006 Ref. No. VP-400
2.75” side viewports	Kurt J. Lesker	VPZL-275
6.0” Groove-grabbers	Kimball physics	MCF600-GrvGrb-C01
Ceramic rods	Kimball Physics	51-537005
Socket receptacles	PSC Electronics	0672-4-15-15-30-27-10-0
RF Feedthrough	MDC Vacuum	9412011
2.75”-1.33” zero-length reducer	MDC Vacuum	150001Ref. No. 275X133
3-pin UHV cable with PEEK socket (female)	Accu-Glass	110651
3-pin power feedthrough (1.33”) for oven and shield	Accu-Glass	110600
4.5”-2.75” conical reducer	MDC Vacuum	402032
4.5” d-sub 2 x 25 pin feedthrough	Accu-Glass	100225
Screw clamp assembly	Kimball Physics	51-313107
D-25 socket PEEK connector (Female)	Accu-Glass	100460
D-25 contacts	Accu-Glass	100180
AWG-22 solid core wire	Accu-Glass	100680
3-way air side connector with socket	Accu-Glass	110704

7.1.2 Socket wiring

The chip socket is wired for 100-pin connections. All wires are 24 AWG (American Wire Gauge) and are Kapton-shielded, solid-core, and acquired from AccuGlass. The wires are compatible with 250°Cbake-out temperatures and UHV operation. Two of the pins are attached directly to the RF and RF-ground feed-through, which is mounted on a flange at the side of the octagonal chamber. The remaining 98 wires are connected to socket pins and are routed to the trap electrodes through carrier connections. These wires are grouped together in four 25-wire groups, referred as "Quad 1" to "Quad 4" in Figure 52. They are routed to four d-sub 25-pin feedthroughs mounted on flanges at two of the octagon side ports as shown in Figure 56. These wires are used to supply compensating voltages to the trap electrodes from the supplies connected on the air side. On Quad1 two pins of the socket are not connected to D-25 pins because these two pins are connected to the RF-feedthrough shown in Figure 56. In Figure 52 only one of the four 25-pin D-connectors is shown. All the connectors have same wiring connection sequence.

7.1.3 Shield

A wire-mesh shield is installed above the trap to avoid the excess micromotion and instabilities caused by the stray fields. The stray fields are typically generated by dielectric charging of the glass windows and other insulating materials in the chamber around the trap. Photoelectrons, driven away from the trap by the negative RF cycle, can charge in-vacuum insulators to the peak RF voltage. It is important to install a ground plane above the trap that shields the trap from these fields. Since laser access for the symmetric trap is through the chip, the shield has pass the laser beams without excess light scattering. During four testing phases, three slightly modified shield designs were used. CAD drawings of these designs are shown in Figure 53. The first three phases used two designs that consisted of the slotted electroformed mesh covering region above the trap while maintaining laser and visual access. Two pieces of the mesh were spot-welded to a metal sheet plate with a gap centered on the trap slot to allow laser beam access free from scattering

from the mesh screen. For one of the designs the mesh plate was installed on a mounting block with screws as shown in Figure 53(a). A mesh mounting block was designed for this system and machined in the GTRI machine shop. In another design the mesh metal sheet was screw-attached to another metal sheet as shown in Figure 53(b). The last phase of the experiment used a top-ground shield design that has no mesh. Without mesh the optical access becomes > 50% open. However the shielding effect decreases. The design shown in Figure 53(c) used in the last phase of trap testing had shielding effect of 16dBV, calculated using BEM modeling. This is an order less in a shielding effect as compared with the mesh-shield design; however it is adequate to prevent excessive stray fields. With the improved optical-access offered by this shield avoids the light-scattering caused by the mesh used in earlier designs. Scattering from the mesh edges can add to the background noise in the collection system resulting in decreased ion visibility. The shield is connected through a wire to one of thee pins of a 3-pin feedthrough on one of the octagon ports. The three-pin feedthrough (listed in Table 12) is 1.33" in diameter requiring a 2.75"-1.33" adapter as shown in Figure 56.

7.1.4 Oven

The oven design was based on ohmic heating in the supporting wires. The mounting is flexible enough that it can be straightened and visually aligned to the slot during assembly. Since the atomic Ca source oxidizes rather quickly, the oven is designed so that it can be installed as a last step before sealing the chamber. A 3D drawings of the oven assembly is shown in Figure 50. Two different oven designs were used for the four experimental arrangements listed in the Table 11. The first three experiments used the design shown in Figure 54(a) and the last experiment used the design shown in Figure 54(b). In the first design the chamber consists of a steel wire inserted through a steel tube. The steel tube is drilled with an approximate 1 mm x 3 mm slit (See Figure 54(b)). The tube is crimped on one end so that it locks against the steel wire. The tube is then filled with powdered Ca metal and the remaining side is crimped to trap the Ca powder in the tube. The oven is

installed by winding the ends of the flexible steel wire onto the oven mount screws. After installation the oven is visually aligned and the screws are tightened. The oven mount screws connect to vacuum feed through wires that are fed through a flange attached to one of the octagon view ports as shown in Figure 56. The oven is heated to produce adequate Ca atom flux by ~2 A of current through the mounting wires.

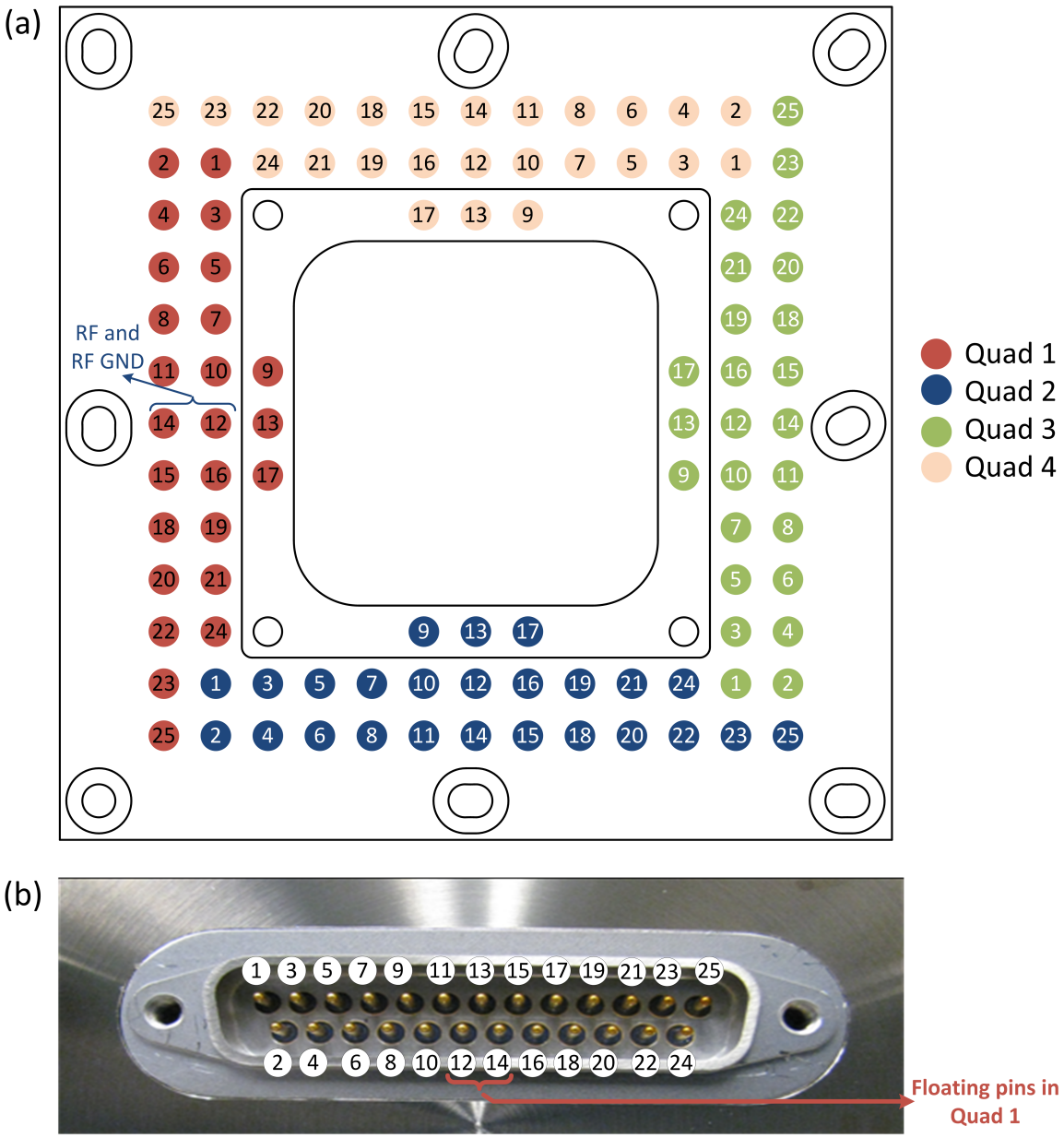

Figure 52: Four quadrants of the socket and pin map of D-25 connector. In (a) each quadrant and its map is laid out which can be mapped into D-25 connector. Only one connector is shown in (b) because all the connectors follow same pin-map for the corresponding quadrant. Only in the case of Quad 1, pins 12 and 14 are connected to RF and RF ground on the socket side and on the D-25 side the pins are floating. For the hardware map from the socket pin to trap electrode see next chapter. For quads position on the UHV system see Figure 56.

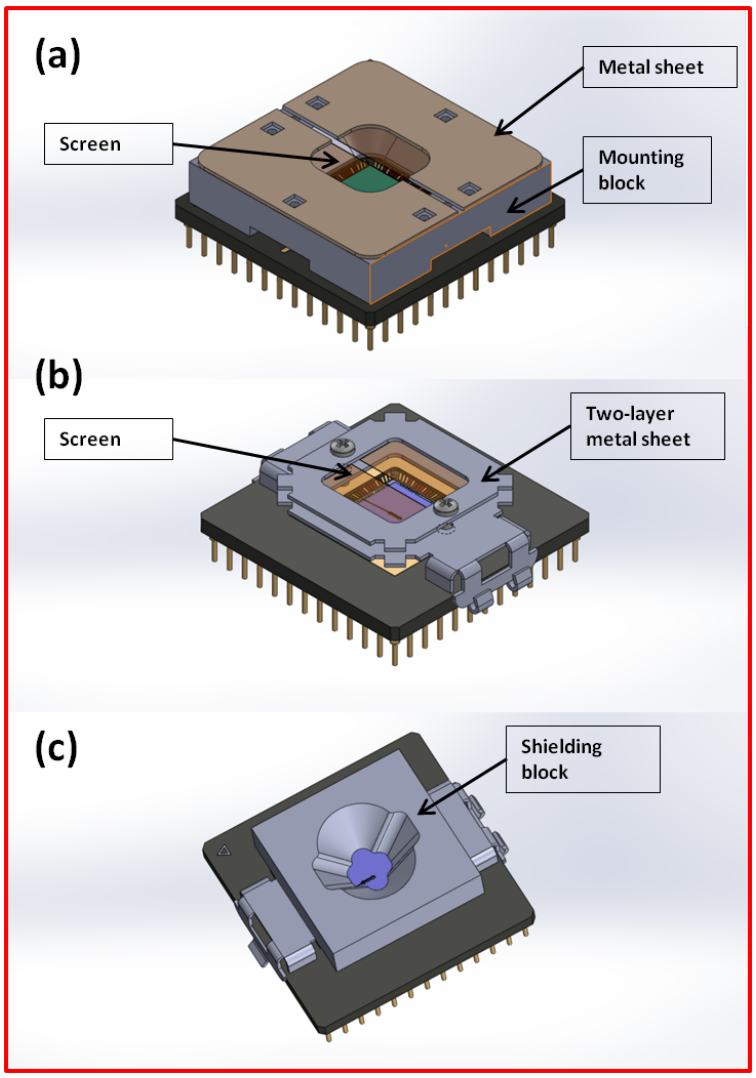

Figure 53: Drawings of the top shield designs used in testing symmetric traps. (a) design was used in first phase of testing, (b) in second and thirs phase of testing (c) was used in last phase of testing (see Table 11 for phases).

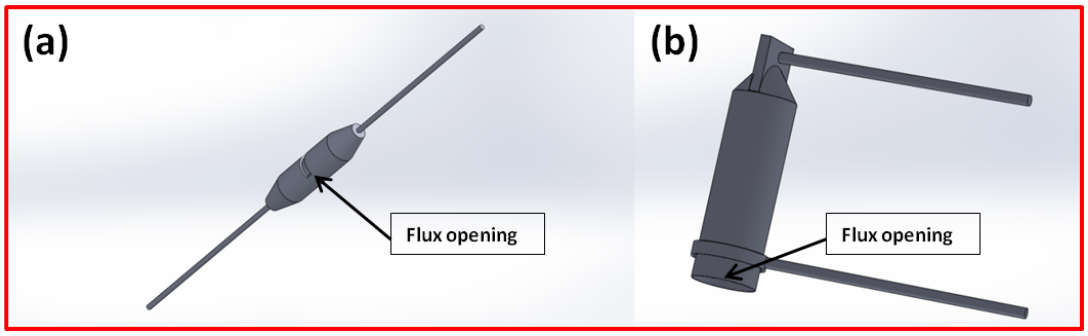

Figure 54: Drawings of the oven design used in testing symmetric traps. First three testing phases (see Table 11) used the oven design shown in (a) and last phase of experiments were performed using the oven design shown in (b).

The oven is outgassed at 2.5 A for ~2 minutes during the bake-out. During the experiment the oven is operated at lower current (typically < 2 A) to form the Ca atomic beam. In the third phase of the experiment, the same oven design was used but it was moved farther from the back side of the trap to install an oven-shield. Because of that the operating currents of the oven were in 2.5 A to 3 A range. The second design of the oven shown in Figure 54(b) has spot-welded wire on the outside of the oven-tube and the one side of the oven-tube is crimped shut and other side of the tube has opening of 1.25 mm radius. The oven is installed at an angle to achieve orthogonality between the photoionization beam and the atomic beam to minimize the Doppler broadening. This arrangement will be discussed in more detail in next chapter.

7.1.5 Oven shield

The angular distribution of the Ca atoms omitted from the oven slit is distributed spatially according to the cosine emission law. The cosine distribution of atoms is directed to center at the ion trap center. However, Ca deposition will form a continuous film on the back side of the socket resulting in shorting the sockets pins to each other. To avoid this undesired deposition, the back side of the socket is protected by a shield. Three different designs were used to shield the oven flux as shown in Figure 55. In first phase of the experiment, a steel foil was used to cover the back side of the socket as shown in Figure 55(a). The steel foil functionally protected the back side of the socket. However, it was not a well-designed component that completely protected the back side. It was replaced with a machined component as shown in Figure 55(b) in subsequent experimental phases. This shield was spatially matched with the oven emission after the oven was moved farther from the back side of the trap and screwed to the back side of the socket base plate. This shield was designed to allow appropriate optical access for the axial and radial laser beams. The oven assembly used in the fourth experimental phase was designed to emit the Ca atoms at a 85°angle to the photoionization beam. The angle close to 90°was chosen to reduce the Doppler broadening of the photoionization beam natural linewidth. To install the oven at

angle on the back side an atomic flux collimating tube was installed at the opening of the oven. The atomic flux passing trough the tube emits at an angle near the trap back-side. A new oven-shield was designed to clamp the collimating tube. The shield shown in Figure 55(c) only holds the shielding tube at an angle to assure that the flux is directed at an angle. This arrangement is discussed in more detail in Chapter 8.

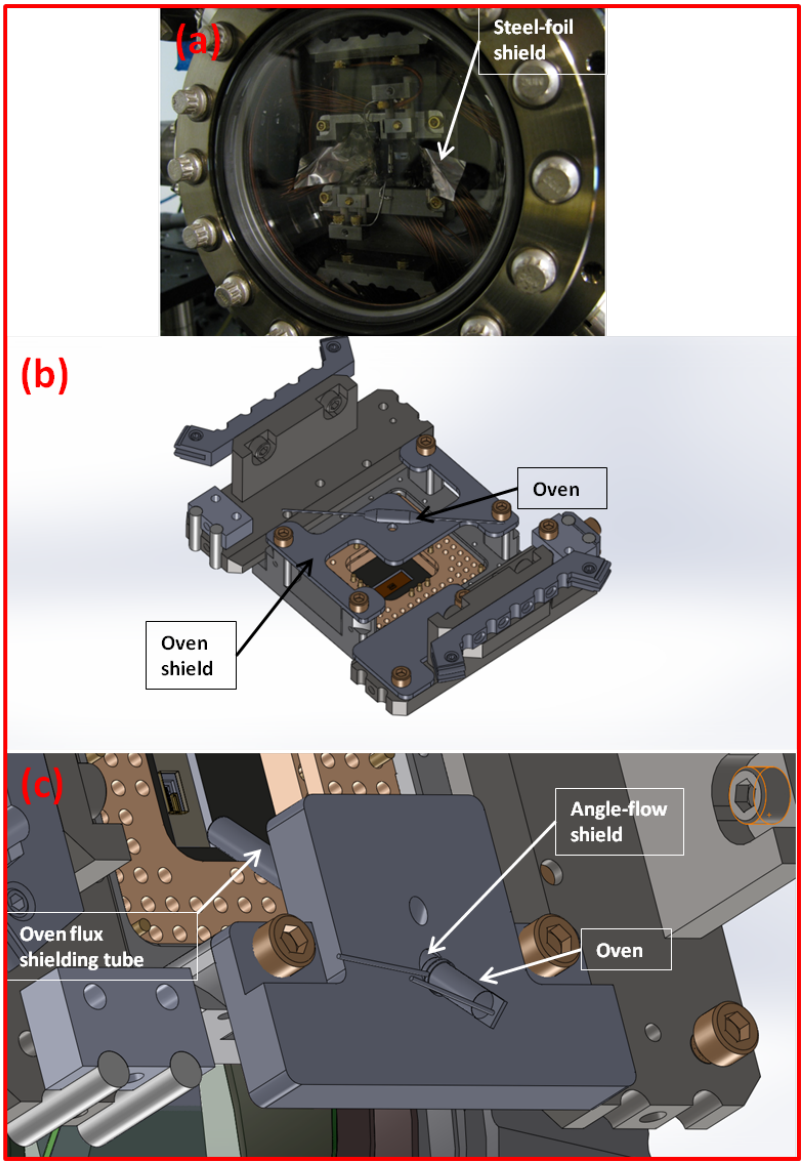

Figure 55: A picture of steel foil used as oven shield in first phase of testing ins given in (a). In (b) and (c) drawings of the oven shield designs are given. These designs were used in testing symmetric traps during rest of the experimental phases (See Table 11).

7.2 UHV system

The main components used in the UHV testing system apart from the chamber itself include pumps, connectors, and shut-off valve. The spherical-octagon chamber has eight 2.75-inch view ports as shown in Figure 56. Two of the ports are connected to 4.5" feedthrough flanges each having two 25-pin D-type feedthroughs. In first phase of the experiment, one port was connected to a leak valve and another port was connected to an ion gauge. The leak valve and ion gauge were removed from the UHV system after the first phase of the experiment because of the uncertainties in operation compatibilities of these devices with the trap operation. These two ports were sealed with blank flange for the remaining phases of the experiments. The fifth port is used to attach an RF feed-through. The sixth port has atomic oven and trap shield 3-pin feedthrough. The seventh port is sealed with a blank flange and the eighth port is attached to an ion pump underneath the UHV system. All of these octagon ports are identified in Figure 56. Since the apparatus is baked at 250°C, all parts have to be compatible with these temperature requirements. To pump down to chamber pressures below 10^{-11} Torr, an additional Ti sublimation pump is attached to the apparatus. A list of the components used in the UHV system is given in Table 13. A description of each apparatus component is given below:

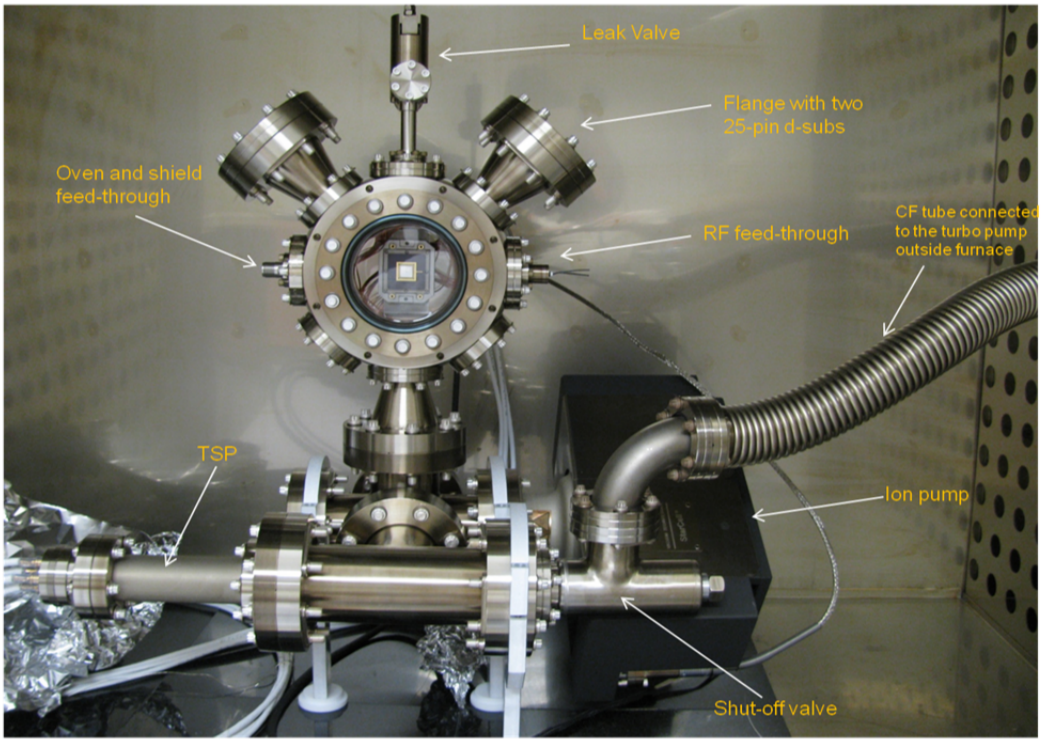

Figure 56: UHV apparatus components. The system in this picture is placed in Blue-M furnace and ready to be baked.

Table 13: List of the external components that are acquired from external vendors to build the UHV system for the symmetric trap testing.

Component	Vendor	Part No.
55 l/s ion pump	Varian	9191340
Fore-line shut-off valve	Kurt J. Lesker	VZCR40R
Leak valve	Kurt J. Lesker	LVM
Ti sublimation pump (TSP)	Varian	9160050
Ion pump controller	Varian	9297000
4.5” six-way cross	Kurt J. Lesker	
TSP nipple	Kurt J. Lesker	

1. Ion pump: The spherical-octagon is attached at the bottom to a four-way cross which has an ion pump connected to one of the flanges. The ion pump is a Varian VacIon 55. The ion pump can be started when the pressure in the system is less than 10^{-3} Torr. The pump can be baked up to 350°C and its pumping rate is 55 ls^{-1}.

2. Titanium sublimation pump (TSP): On one of the flanges of the six-way cross that is attached to the octagon, a Tee-flange is connected. On one of the sides of this

Tee flange, the TSP is attached (Figure 56). The TSP used in this setup is a filament-based cartridge Varian 9160050 with three filaments. Each TSP filament is outgassed during the system bake-out at 35 A for 3 minutes. Only one of the filaments is fired-up at 46 A for 1.5 minutes for chamber pumping. Typically the TSP is fired-up when the pressure is already in order of 10^{-9} Torr. The TSP coats the system walls with Titanium (Ti). Ti is considered to be a good "getter"; it absorbs residual molecules in the UHV chamber.

3. Leybold ion gauge: This system is equipped with an UHV ion gauge that can read down to 1.5 x 10^{-12} Torr. The gauge is Leybold Ionivac IM 540 with IE 514 sensor. The gauge can be operated at a high temperature and is attached to one of the view port flanges of the octagon. It is encapsulated in a short nipple that maintains the filament at some distance from the trap and yet the relative small size of the gauge and low temperature allows it to be mounted close to the ion location for more accurate monitoring of the relevant pressures.

4. Leak valve: To perform ion lifetime experiment the system is equipped with a leak valve that can be utilized to vary the ion collision rate with various gases. The leak valve is supplied by Kurt Lesker with LVM series. Its operating pressure is within the range of 10^{-11} Torr. Its closed leak rate is 10^{-12} Torr per second.

5. Fore-line shut-off valve: The shut-off valve is attached to the second Tee-flange face. This valve is the main shut-off valve that seals the system from the air side. The valve is open when the fore line is attached and is being pumped through a roughing and a turbo pump. Once the appropriate pressure is reached and bake-out is completed, this valve is sealed and the fore-line is disconnected. The valve is supplied by Kurt Lesker Nupro under the name of "B-series". It is specified for high temperature and UHV applications.

6. Roughing and Turbo pump: Even though the roughing and turbo pumps are not parts

of the system, they are attached when the system is being pumped down and baked-out. The roughing pump brings the pressure down to 10^{-3} Torr and then the turbo rotors are started that pump the system down to the 10^{-7} Torr. These pumps are part of same package and supplied by Varian with the TSP Bench label.

After the octagon and system is assembled the UHV system is baked at hight temperature. The bake-out procedure has been developed at QIS lab based on several years of experience and consultation with other leading ion trapping and experimentalist groups. The procedure insures that the entire equipment is utilized at its optimal operating performances within the experimental requirements. The procedure is as follows:

1. After the conflate flanges (CF) of the UHV system are tightened and the system is leak checked, the trap is tested electrically on the air side. This testing typically includes measuring the capacitances of the DC electrodes the RF electrode of the trap, the oven and the shield connections. Once all possible and necessary electrical verifications are done, the system is moved into a large oven where all the cables for the TSP, ion pump, and oven are laid. The CF tube connecting to roughing/turbo pump is arranged so that the oven can be closed. The furnace is a Blue M series with a programmable controller.

2. The roughing pump is started with the shut-off valve open and, once the pressure is in 10^{-3} Torr range, the turbo pump is started. Once the pressure is in the 10^{-5} Torr range the oven is started and ramped up at 1°C per minute to 200°C.

3. The furnace is kept at 200°C for eight hours and then ramped down to 180°C.

4. The system is maintained at 180°C for 54 hours or until the pressure reaches a steady state.

5. The atomic oven and TSP pumps are outgassed during the bake-out. The atomic oven is outgassed at 1.5 A for 2 minutes and then 2.5 A for 2 minutes. Each filament

of the TSP is outgassed at 35 A for 3 minutes.

6. Once the pressure has stabilized, the ion pump is started. The pressure is monitored until the pressure readings of the fore line gauge and ion pump gauge are nearly equal.

7. The oven temperature is ramped down at 1°C per minute to 60°C.

8. As soon as temperature decreases to 60°C, the shut-off valve is sealed at a specified 65-in-lb torque. At this and at that time the turbo and roughing pumps are turned off.

9. Once the system is cooled completely and the pressure is in low 10^{-9} Torr range one of the TSP filaments is fired up at 46 A for 1.5 minutes and the system is left at room temperature for at least 12 hours to observe the pressure descends to the 10^{-11} Torr range.

7.3 Experimental setup

After the UHV system is baked and a pressure less than 2.0x10^{-10} Torr inside the chamber is achieved, the system is moved to the optics station. Before it is moved, capacitance measurements of each DC electrode are taken again to ensure that the bake-out process did not cause any short to ground or internal electrical disconnect. The optics station provides the laser beams for photoionization, cooling, and re-pumping. There is also an RF generator and helical resonator used to drive the RF trap electrode. The resonator matches the impedances from the source (50 Ω) to the capacitive RF electrodes ($\sim$ 12 pF) to minimize the RF power requirements. DC compensating voltages, controllers, and imaging optics are also available at the optics table. All of these components are discussed briefly in following sections. The outline of the experimental setup is shown schematically in Figure 57.

7.3.1 Laser layout

The atomic beam from the Ca oven passes through the trap slot and is irradiated by two photoionization laser beams. As shown in Figure 57, the two photoionization laser beams propagate from the same optic fiber. A laser beam with a wavelength of 423 nm excites the dipole transition from neutral ground state of 4^1S_0 to 4^1P_1 state. A second laser with a wavelength of 377 nm excites the transition from 4^1P_1 to the continuum and completes the photoionization process. The ^{40}Ca-level scheme and ^{40}Ca-energy level diagrams are shown in Figure 59.

In the first three phases of the experimental setup, the lasers propagate through the trap slot at approximately 30° with respect to the normal to the trap surface. The photoionization laser beams (both the wavelengths 423 nm and 377 nm) are coupled into the same fiber. The combined beams exit the optic fiber and are guided towards the vacuum chamber with mirrors. The lasers are focused through the trap slot and aligned to minimize scattering from the slot edges. The focal-mode diameter at the trap slot is approximately 20 μm and the slot width is 125 μm . As the atomic oven generates neutral atom flux, the fluorescence due to the 423 nm transition can easily be observed on the CCD camera viewing the slot region. With sufficient atomic flux at an oven current near 2.6 A the 423 nm fluorescence was observed. The resonant frequency was measured to be 422.79211 nm (354.53885 THz) with a Doppler broadening of 1.2 GHz. This Doppler broadening is due to a wide angle (135°) between the atomic beam and the photoionization beam.

In addition to the photoionization fluorescence lasers, the ion cooling with lasers wavelengths of 397 nm and 866 nm for $^{40}Ca^+$, are guided to the trap slot by mirrors and beam splitters. These lasers are co-aligned and directed to the trap slot at $\sim 40°$ to the plane of the octagon face from the side opposite the photoionization laser beams . As shown in Figure 57 all of the laser beams are propagating toward the front surface of the trap. All laser beams must overlap exactly at the ion position to within 10 μm to ensure ion trapping.

Bringing the beams onto the front trap surface, where the camera primarily sees backscattered radiation only from the trap surface, allows much more accurate beam alignment than using propagation from the backside of the trap where there is no camera access. As shown in Figure 59 the $^{40}Ca^{+}$ cooling transition $4^2S_{1/2} \leftrightarrow 4^2P_{1/2}$ is at a wavelength of 397 nm and the re-pumping transition $3^2D_{1/2} \leftrightarrow 4^2P_{1/2}$ is at a wavelength of 866 nm. These two lasers use the same focusing lens as they propagate toward the trap. As shown in Figure 57, a dichroic mirror is used to combine the 397 nm laser beam by reflection and 866 nm laser by transmission.

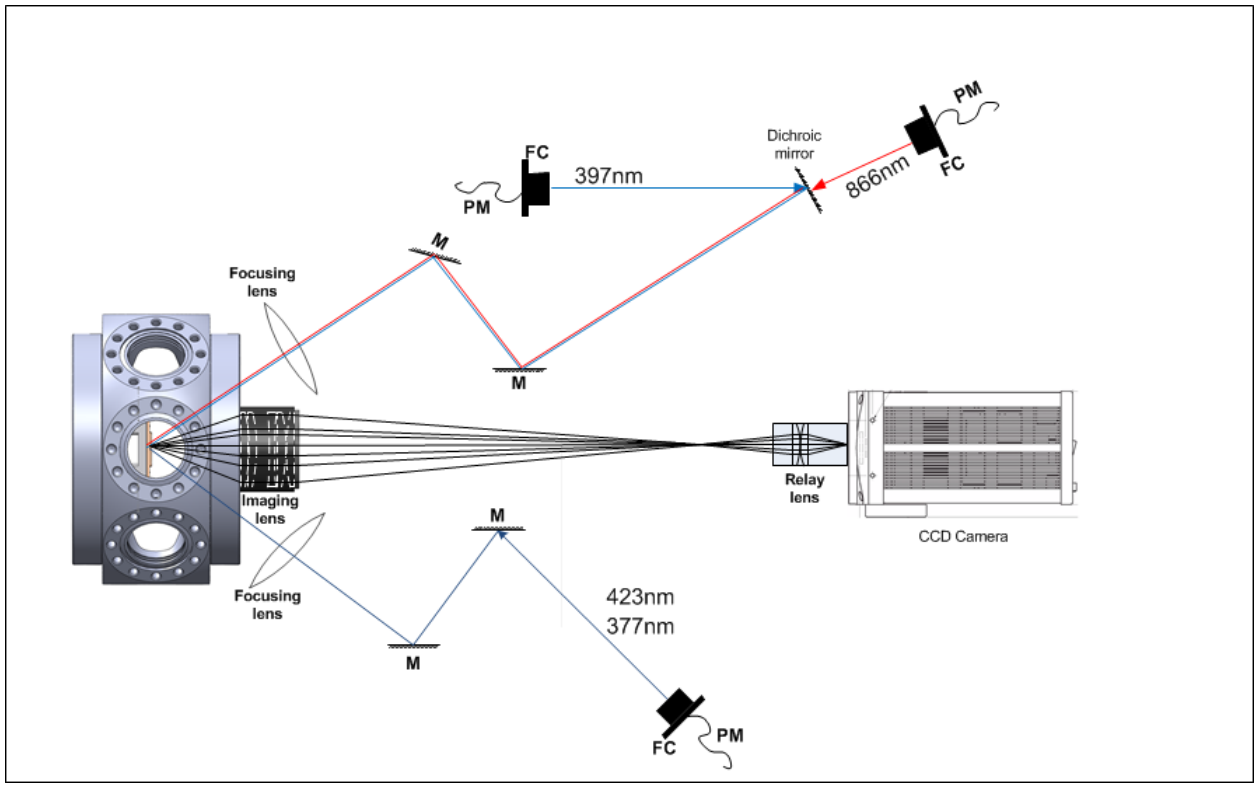

Figure 57: A top view of the layout of the lasers and trapping chamber. The 423 nm and 377 nm lasers are fiber-coupled, the 397 nm and 866 nm enter from the other side of the trap at roughly an angle of 30°. The imaging lens (NA~0.4 with x10 magnification) is mounted in a tube right in front of the trap outside the window. M is for mirror, FC for fiber coupler, and PM is for polarization maintaining fiber.

For the micromotion compensation and optimization of the ion cooling, the frequency of the cooling beam (397 nm) has to be shifted within a few tens of MHz to the low frequency side of the 397 nm resonance line center. To achieve this frequency sweeping, an

acousto-optic modulator (AOM) in a double-pass configuration is used. The double-pass configuration avoids beam alignment problems caused by angular sweeping of the AOM that accompanies the frequency sweeping. The double-pass configuration compensates the angular beam deflection since the laser passes through the AOM twice. This results in twice the frequency shift. The AOM used in this experiment is Brimrose Corporation model number TEF-220-100-.397. The substrate of this crystal is tellurium dioxide (TeO_2) and each pass results in a frequency shift 200 MHz. A schematic drawing of the double-pass the AOM configuration with cooling beam is shown in Figure 58.

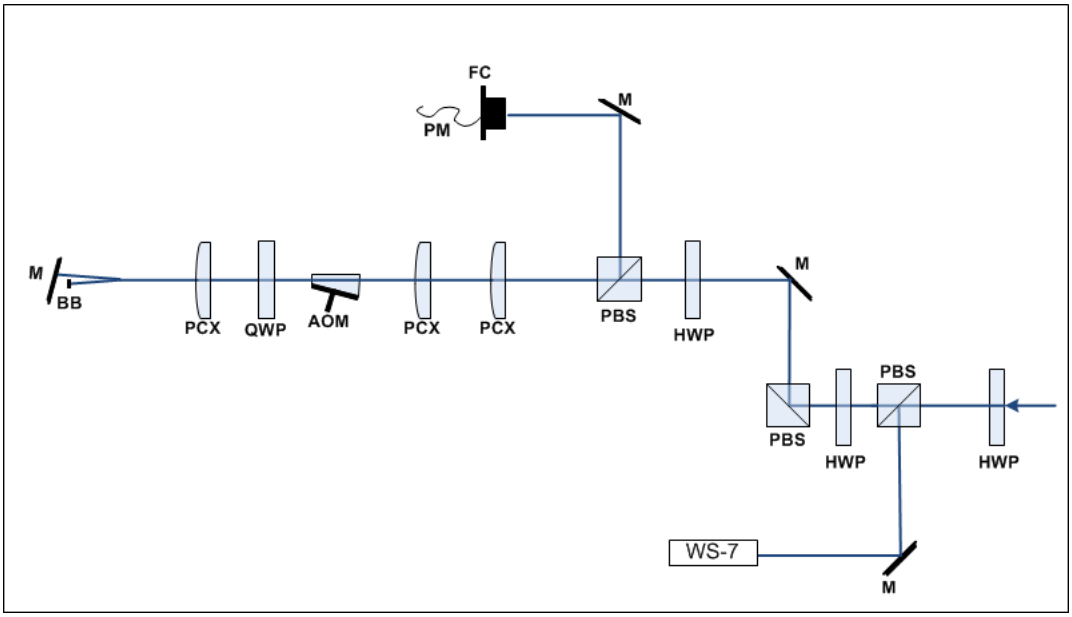

Figure 58: A schematic drawing of the double-pass configuration of the AOM for cooling beam. The components are labeled; M: mirror; PCC: plano-concave lens; PCS: plano-convex lens; PBS: polarizing beam splitter; QWP: quarter-wave plate; HWP: half-wave plate; FC: fiber coupler; PM: polarization maintaining fiber; AOM: acousto-optic modulator; BB: beam block; WS-7 is optical switch.

In the last phase of the experiment, the trap was rotated 90°and the oven was reoriented to reduce the effective Doppler broadening of the atomic beam. The new arrangement required the 423 nm and 377 nm beams to enter the trapping region at an angle of 45° to the plane normal to the trap surface in a plane vertical to the optical table. As a result another level of optical plate (bread-board) was added so that the ionization beams can be brought in at a vertical angle. The details of this arrangement will be discussed further in

next chapter.

7.3.2 Collection optics

The CCD camera (Photometrics Cascade 1K) has 1004x1002 resolution with 8 μm pixel size and 62 % quantum efficiency. The imaging lens system was designed at GTRI. The lens has numerical aperture of 0.4 and a limiting resolution for ion imaging of 4 μm with the magnification of 10. The primary objective lens is a compound lens designed of a concave lens sandwiched between two plano-convex lenses on each side. This lens magnifies the object (ion) and produces an image approximately 12-inch from the trap surface. A relay lens, a compound lens composed of two plano-convex lenses, relays the magnified image from the primary lens to a CCD camera that is positioned 16 inches away from the trap surface. The schematics of the collection optics are drawn in Figure 57.

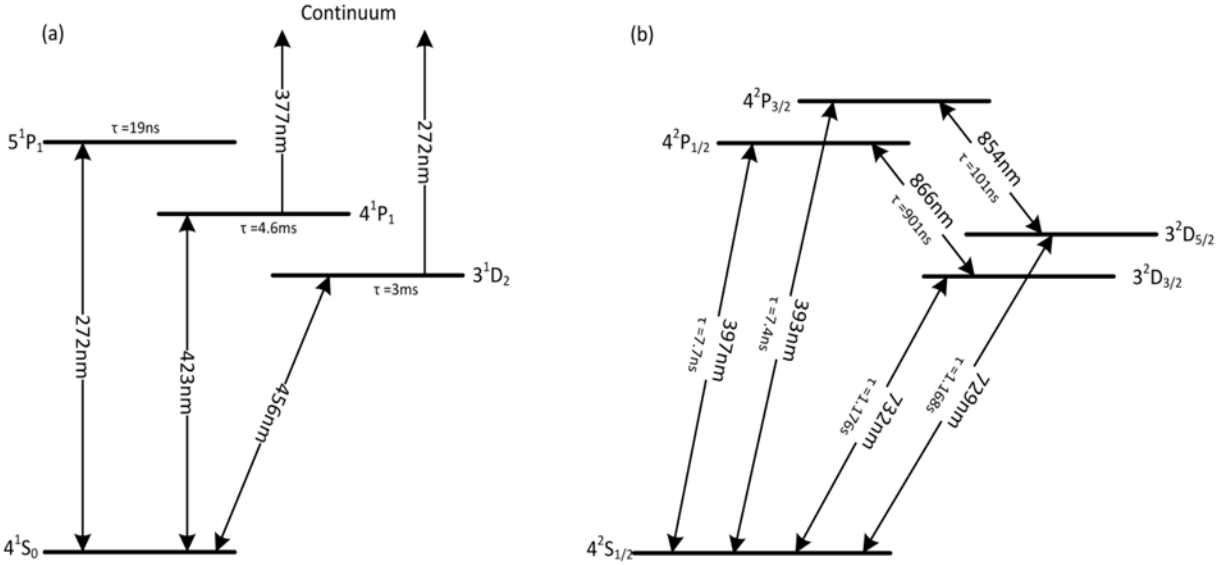

Figure 59: ^{40}Ca level scheme and energy-level diagram. (a) ^{40}Ca photonionization to continuum using 423 nm and 377 nm lasers (b) cooling transition of 397 nm and repumping 866 nm transition.

7.3.3 RF resonator

An HP 8656B RF source is used to drive the trap RF at a typical frequencies in the 40-100 MHz ranges. To reduce the noise injected into the RF trap circuit and minimize the source power requirements, a RF resonator (LCR helical resonator) is used to match the

impedance between the circuit elements at the trap side and the air side. A schematic diagram of the helical resonator attached to the UHV system station is shown in Figure 60. On the air side a RF signal generator and amplifier with 50 Ω impedances are used to generate a signal at the resonant frequency of the resonator. The resonator is designed to match the trap capacitive impedance near 12 pF (including the wire and fan-out to the 50 Ω source). The resonator was designed to have an unloaded quality factor Q=200 at 70 MHz and Q=60 at 40 MHz. With the 12 pF trap load, the resonator has Q=120. The resonator was designed to have the resonant frequency ∼60 MHz for the first two phases of the experiment. With the trap load the measured resonant frequency was 65.05 MHz in these cases. For the third and fourth phases of the experiments to test the trap of generation **B** the resonator was modified to be operated at ∼ 40 MHz. If the output impedance is not matched to the input much of the power will be dissipated or reflected from the trap. An RF amplifier can induce noise, causing ion heating [88]. The helical resonator not only provides the impedance matching, but also filters out noise at the ion motion frequencies near 1 MHz. With the resonator in place, the voltage at the trap is calibrated using a capacitive tap on the helical resonator coil to measure a voltage that is correlated with the trap electrode voltage measured with a low capacitance high voltage probe (Tek P5100). The appropriate trap voltage (e.g. V_{pp} =180 V at 70 MHz and V_{pp} =60 V at 44 MHz) is then set using the tap voltage measurement while the frequency is tuned to the loaded resonator frequency.

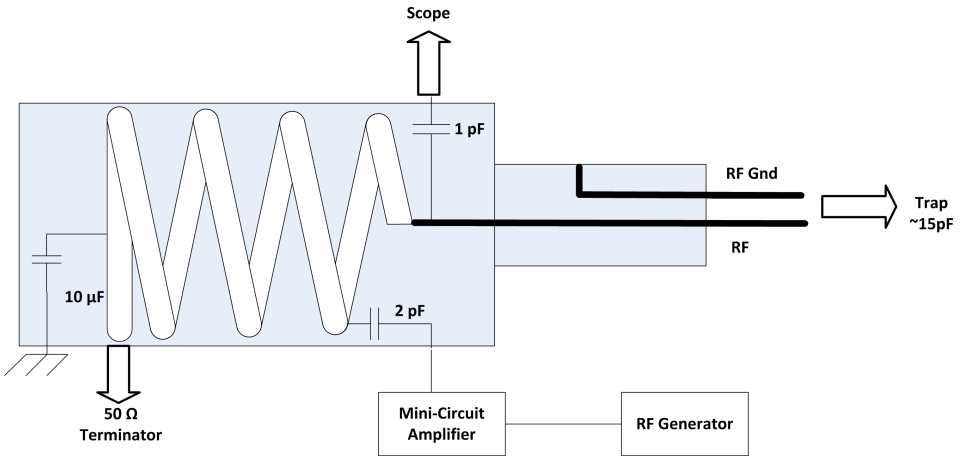

Figure 60: RF resonator connected to the UHV system's RF feed-through. Resonator is a helical cavity LRC circuit. It filters amplifier noise and matches impedance to minimize the power dissipation through trap elements. RF generator used in the experiment is HP 8656B signal generator with the Mini Circuits amplifier TIA 1000-R8

7.3.4 DC voltage supply

A multi-channel data acquisition and control platform is used to supply compensating DC voltages to the trap DC electrodes. DC voltages are required to be within the range of +10 V to -10 V. For that pupose, a multi-channel analog output PXI 6733 cards were used from National Instruments (NI) along with chassis model 1042. Each PXI-6733 is a high speed analog output card with 8 digital I/O channels that can operate at a 10 MHz clock rate with 16-bit resolution. Six of these cards were used to control 40 electrodes. In-house coded software was used for voltage control and waveform generation. The software is written to control FPGA-based and TTL-based data acquisition systems as well. The software is written in Igor language and calls NI proprietary APIs to send voltages triggered by internal clocks. DC voltages applied to the DC electrodes are low-pass filtered using multi-channel boards that are attached in series with supply cables. These filters have RC components laid out on PCB boards. A simplified circuit diagram of the low-pass filters is shown in Figure 61. These filters provide a ground for the RF potential that couples to the DC electrodes through the inter-electrode capacitance. Inter-electrode capacitance (<1 pF) is much lower than the capacitors (20 nF) used in the RC filters providing a lower impedance path. The cutoff frequency of the circuit is a KHz. The frequencies below a KHz go through

the trap (applied DC voltages) and any RF pick-up at higher frequencies is filtered out.

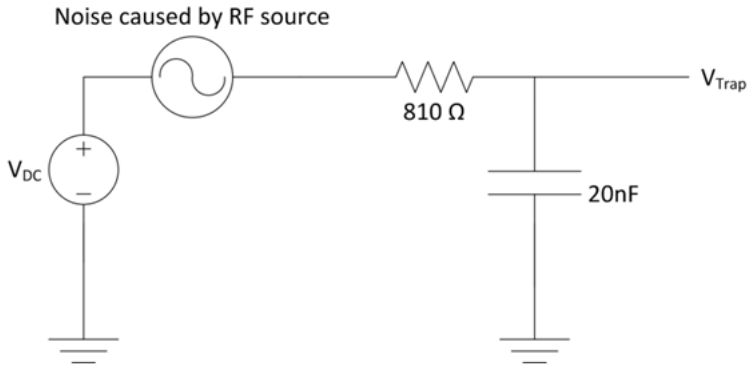

Figure 61: Simplified circuit representing noise from the RF source being filtered out by the RC filter.

CHAPTER 8

MONOLITHIC SYMMETRIC ION TRAP : TESTING AND RESULTS

The testing of two generations of the symmetric traps, generation **A** and generation **B** was conducted between October 2011 and October 2012. One symmetric trap chip from a wafer of generation **A** and two trap chips from two wafers of the generation **B** were tested. Additionally, to verify the UHV system built for testing the symmetric traps, a surface-electrode trap , "Gen III", was tested [89]. All of this testing was conducted in four experimental phases which are listed in the Table 11 given in Chapter 7. The fabrication of the first generation **A** symmetric trap was completed in October 2011. In the first three experimental setups the trap slot was parallel to the optics table. The cooling and photoionization lasers were aligned to pass through the center of the trap slot (see Figure 22). Preliminary testing of these initial traps proceeded through November and December of 2011. Two generation **A** symmetric-trap chips were packaged and loaded into the UHV chamber and a complete testing station was assembled. A Ca oven was installed and fluorescence from the atomic source atoms was demonstrated. The laser system was tuned for trapping conditions and the trap voltages required were applied to the trap; however, no trapped $^{40}Ca^{+}$ ions were observed. There were uncertainties in the laser alignment and collection optics during this initial testing. To optimize all parameters of the testing system, a well-characterized surface-electrode trap called "Gen III" was loaded into the UHV chamber in the second experimental phase. After optimizing the laser alignment and light collection systems, $^{40}Ca^{+}$ ions were trapped in the Gen III trap during January-February 2012, verifying that all parameters are now set properly for ion trapping attempts in the symmetric trap. In March 2012, fabrication of generation **B** traps was completed and successful $^{40}Ca^{+}$ ion-loading experiments followed through October 2012. The trap packaging and the results of electrical and experimental testing of each of the setups are discussed in the following

sections.

8.1 Packaging

After completing all structure-related processing steps on the trap wafer, the wafer was metalized with 300 Å Ti and 1 μm of gold (Au) on the back side for packaging. The back-side gold reacts with the solder to form an eutectic bond. The solder composition is 80:20::Au:Sn. To prevent the electrodes on the back side of the trap from being exposed to evaporated Ca and possibly being shorted by deposited Ca, a masking spacer is required between the atomic oven and the trap. The masking spacer was designed and fabricated by processing a Si wafer. The through-wafer slots were etched using dry plasma reactive ion etching (RIE). The spacer dimensions and mask layout are shown in Figure 62.

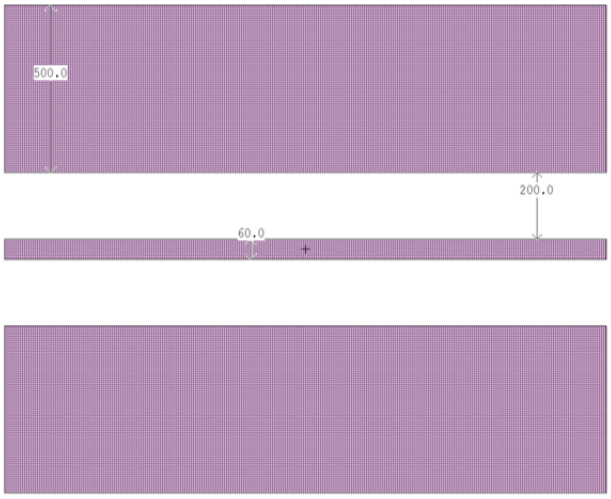

Figure 62: The masking-spacer layout and its dimensions. The 60 μm slot is aligned to the trap slot; the 500 μm slots are for oblique laser access from the back side.

Since the spacer and carrier are to be soldered together, the spacer was also coated with Ti/Au layers. Most of the traps built at GTRI are packaged with the CPGA (PGA10047002) carrier. It is a standard 100-pin ceramic carrier with gold-coated pads and a chip-bond surface. A schematic drawing of the packaging layers is shown in Figure 63. The carrier is laser machined to have an opening for the back-side atomic beam and laser access. The opening can be seen in Figure 63. The carrier was laser machined by an external vendor.

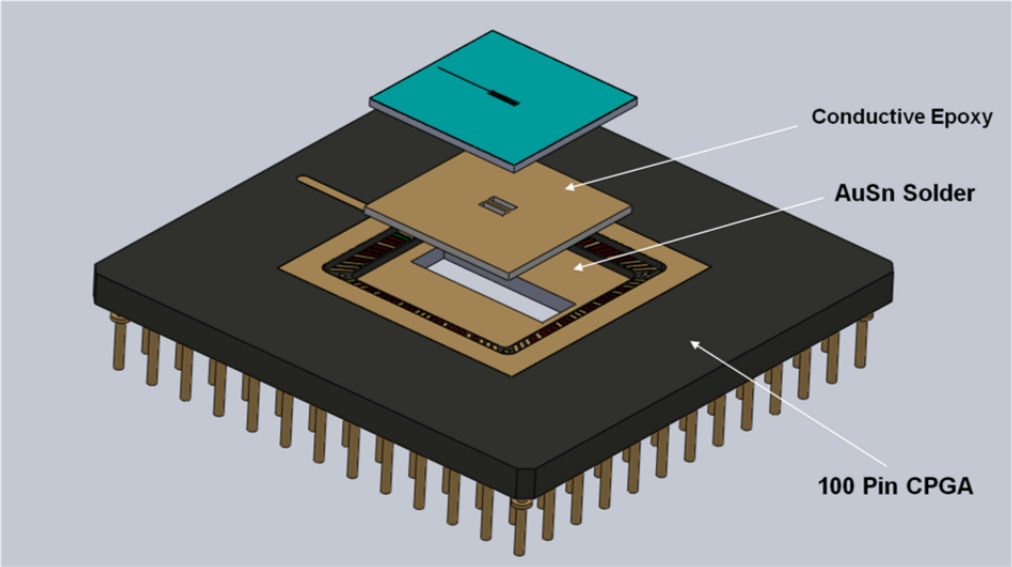

Figure 63: 3D model of the trap packaging layers. Trap is epoxy adhered to the masking spacer and spacer is soldered to the carrier.

8.1.1 Chip bonding

To prevent the trap back-side electrodes from being shorted by evaporated Ca, the masking-spacer slot width must be smaller than the width of the trap slot. Therefore, the slot of the masking trap has dimensions of 1800 μm x 60 μm as compared with the slot of the trap which measures 1900 μm x 125 μm . These dimensions require accurate alignment of the trap and spacer slot to within ~5-10 μm . The solder-bonding process does not allow any alignment time since as soon as the solder flows and the chip is stirred, the bond is developed and the chip locks to that position. To align the masking spacer and trap slots, epoxy bonding allows time for manual alignment during the packaging. To meet this alignment requirement, a silver-filled epoxy (EPOTEK H21D) was used. This epoxy is suitable for UHV applications. The chip-bonding process used for trap packaging is given below:

1. The cleaned carrier is wire bonded at two corners, as shown in Figure 64. These wire bonds insure that the spacer is conductively connected to the ground carrier pads. Since the bottom of the trap chip is to be bonded with epoxy, there could be voids causing intermittent disconnects especially during the UHV system high-temperature

bake-out. Two dummy chips packaged with this process went through standard bake-out. Electrical probing showed intact connectivity between the carrier ground pads and the bottom of the spacer for these baked chips. The wire bonds were still added as redundant connections.

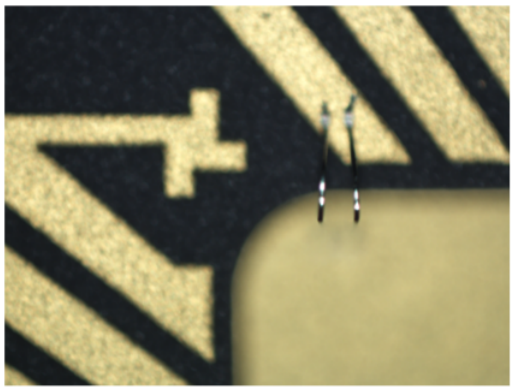

Figure 64: Micrograph of corner wire bonds on 100-pin CPGA. Wire thickness is 25 μm .

2. The spacer was solder-bonded to the carrier using AuSn solder. The spacer is manually centered in reference to the walls of the carrier. A packaging station, equipped with a microscope, a camera, and micrometers, was used for finer alignment. Since the AuSn solder flows at 287.5°C, the packaging assembly was calibrated to achieve the flowing temperature at the carrier by setting the hot plate at 425°C. The packaging assembly has a nitrogen-blowing gun, which achieves immediate cooling of the solder as soon as it is locked after forming the bond.

3. To bond the trap chip to the spacer chip, a conductive silver-filled epoxy (EPOTEK H21D) was used. The conductive epoxy was chosen to make sure that the trap substrate, which is grounded through the carrier, is electrically connected to the spacer. This epoxy has high operating temperature specifications (-55°C to 350°C) and meets NASA outgassing standards, i.e. less than 1 % total mass loss at 100°C. This standard makes it compatible with UHV applications. A couple of dibs of epoxy were applied to the trap chip and the trap was aligned manually under the microscope so that the trap slot was aligned to the center slot of the spacer. The epoxy was cured at

150°C for one hour. The packaging and relative alignment of the trap and spacer is shown in Figure 63.

8.1.2 Wire bonding

Wire bonding of the trap to carrier pads was accomplished using a wedge wire bonder available in the QIS laboratory. This automatic wedge wire bonder is a Model 2470 made by Hugher Technologies. A new wire-bonding program was written for this trap layout. Since the symmetric trap uses a Si spacer with the thickness of 480 μm as compared with the surface traps that are packaged with alumina machined spacers with the thickness of 1.25 mm, the loop height and other wire-bonder-tip-related parameters were modified to wire bond the symmetric trap. Each electrode was double wire bonded with the corresponding pad. The remaining pads were wire bonded to a metallic carrier ring, a part of the CPGA to implement a common ground connection. The wire-bonding layout is shown in Figure 65, and a wire-bonded trap is shown in Figure 66. Each wire bond is 25 μm thick Al wire. As shown in Figure 65, a jumper connects both the trap ground layers M1 and M4 with a common ground around the carrier ring.

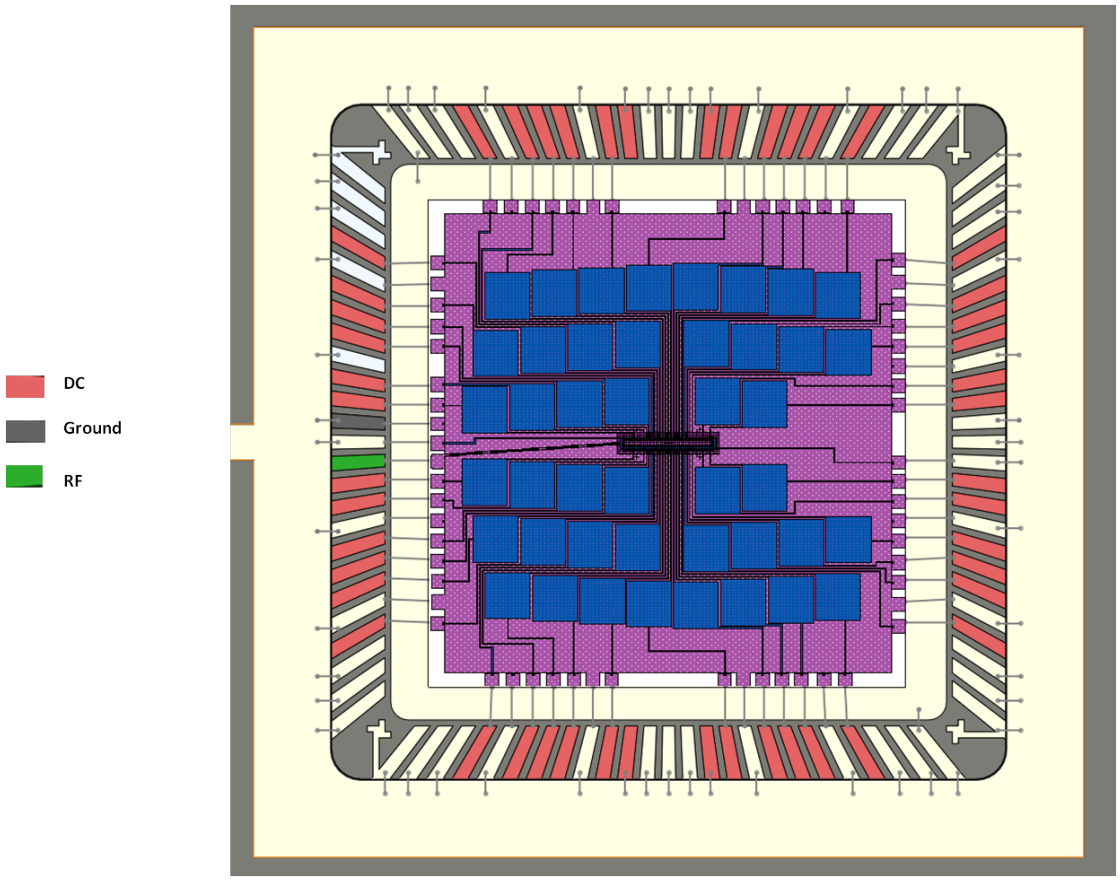

Figure 65: Schematics of the wire-bonding layout of the symmetric trap on 100-pin carrier.

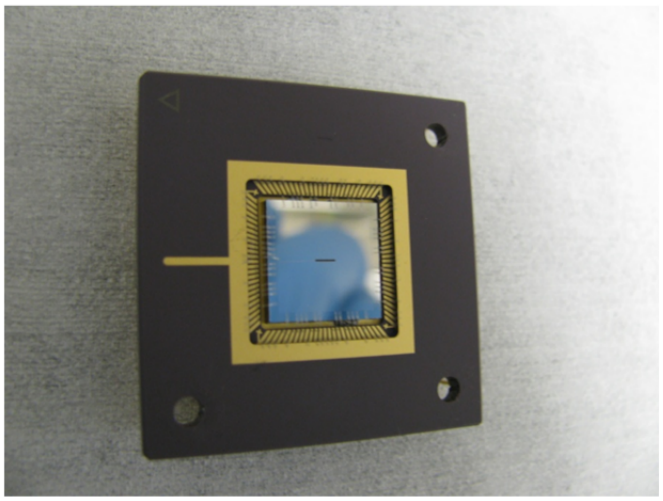

Figure 66: Photograph of packaged symmetric trap of generation A . Trap chip is 11 mm x 11 mm.

8.2 The generation A symmetric trap testing results

8.2.1 Trap electrical testing

Generation **A** trap fabrication was completed in September 2011. A completely processed 100 mm diameter Si wafer of the symmetric traps has 38 trap chips that can potentially be cleaned and tested. Initially, after cleaning five chips, each chip was probed for electrical discontinuity between the RF and DC electrodes and the ground layers. Some chips have a few DC electrodes shorted to ground. Those unintentional grounds could be related to defects in the etching processes that are local to some areas. They could also be an indication of the need for improvement in the etching and the post-processing cleaning steps. Out of the five chips, three traps were packaged and wire-bonded. After wire bonding, the capacitance of each DC and RF electrode was measured. At this point the capacitance measurements include the capacitance of the wire bonds and carrier pads. As discussed in Chapter 7, each trap has on-chip capacitors which are expected to be the dominant capacitive circuit elements for all DC electrodes. As a result, all of the DC electrode capacitances should be approximately same, within the measurement error. The results of the capacitances measured for three chips are shown in Appendix Table 17, where the shorted DC electrodes are highlighted. During these measurements, one electrode of each tested trap consistently was found to have lower capacitance than the others, indicating two possible problems: 1. This electrode has no connection with the on-chip capacitor or 2. It is shorted to a floating-metal component in the structure. After careful study of the mask, it was determined that layer 2 of the mask that creates the pattern of electrodes and on-chip capacitors, had a 2 μm disconnect that caused the bond pad associated with this electrode (identified as 43 in "Carrier Pad" column in Appendix Table 17) to be disconnected. The measurement in this case included the capacitance of the bond pad, carrier pad, and wire bond. This also meant that the electrode connected to pad 43 was floating metal near the trapping region. This is known to cause a variable "stray" field that is difficult to compensate with the other electrode voltages. The capacitance measurements of selected chips that do not have

electrode 43 open are listed in Appendix Table 17. The absence of the defect in selected chips can be explained by the fact that a 2 μm defect in the mask is small enough that there is some chance of it not being resolved during photolithographic UV exposure and development processes of the M2 level. There are some DC electrodes shorted to ground as highlighted in the Table 17. The compensating voltages can be calculated using the electrostatic model considering these shorted electrodes. Only the shorted DC electrode has to be properly grounded so that all the fields on that electrode fuse to ground as well.

8.2.2 Trap testing results

Using the apparatus described above, the generation **A** of symmetric trap was tested. Several chips from this wafer were tested electrically. Only two chips were tested inside the UHV system for trapping, unfortunately without success. Several problems were identified during this testing. These problems are resolved in the generation **B** symmetric traps. The details of each problem, the procedures adapted to test the trap chips and the results are discussed as follows:

1. There was an error in the initial mask design resulting in a 2 μm open space on one of the electrode-connection strips. This error was found during electrical characterization of the trap. Since the photolithography process has a critical dimension requirement of 4 μm , not all the chips have this problem. There are roughly 20 % chips that do not have this problem. These chips were tested electrically for further qualification and two were used for ion trapping tests. The defect is shown in Figure 67.

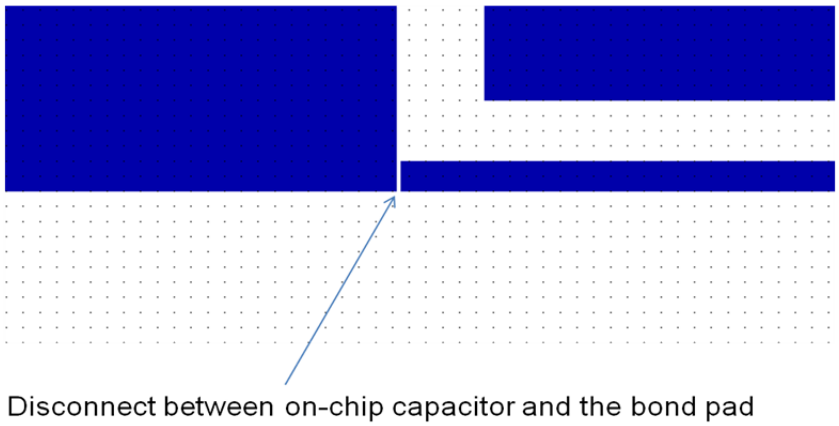

Figure 67: Defect (~ 2 μm) in the M2 layer mask causes a floating electrode.

2. When the first chip was installed and baked, all the lasers were aligned and guided in from the back-side of the chip. The laser overlap was not directly observable by camera due to laser scattering over the back portions of the trap and oven shield. During several initial searches, neutral atomic fluorescence was not observed. During the effort to find the atomic-oven-current required to observe the atomic resonance, the oven flux coated the back side of the socket and as a result the carrier pins were shorted to each other. The conducting Ca coating could be oxidized resulting in a insulating coating by venting the system to air. To prevent this from happening again, a steel-foil-based shield was installed on the back side of the socket after opening the system. The shield covers all the pins and still avoids any contact with any of the oven element. The shield is shown in Figure 55(a) in Chapter 7.

3. Once the system was vented and all Ca oxidized, it was verified that the DC electrodes were not shorted to each other. During the electrical testing it was determined that, intermittently, the DC electrodes were being measured as shorts to ground. After examining the chip surface carefully, several Al whiskers were observed which were grown at the baking temperature of 200°C. This phenomenon is well known and was also seen in our laboratory with previous traps [90]. However, it was previously observed at higher temperature (250°C). These traps went through different finishing

processes than the previous surface traps. The symmetric trap did not go through the last step of oxide etching that passivates the metal surface. It was concluded that since the symmetric trap did not go through this passivation, whiskers were formed at a lower temperature. The next symmetric trap chips went through nitrogen annealing at 200°C in air and the bake-out was conducted at lower temperature (150°C). This procedure corrected the whisker problem.

4. A second trap chip was found without the 2 μm open defect (i.e. a floating DC electrode). It had a thin layer of unknown material spreading along RF rail and adjacent DC electrodes (see Figure 68). This thin layer did not cause shorts between the DC electrodes and the RF rail. However, if this is dielectric material (very likely), it could charge to high voltage from the applied RF voltage and may strongly distort the trapping field due to its close proximity to the trapping region. This trap was installed and trapping searches continued for several days with various compensating voltages without any successful results.

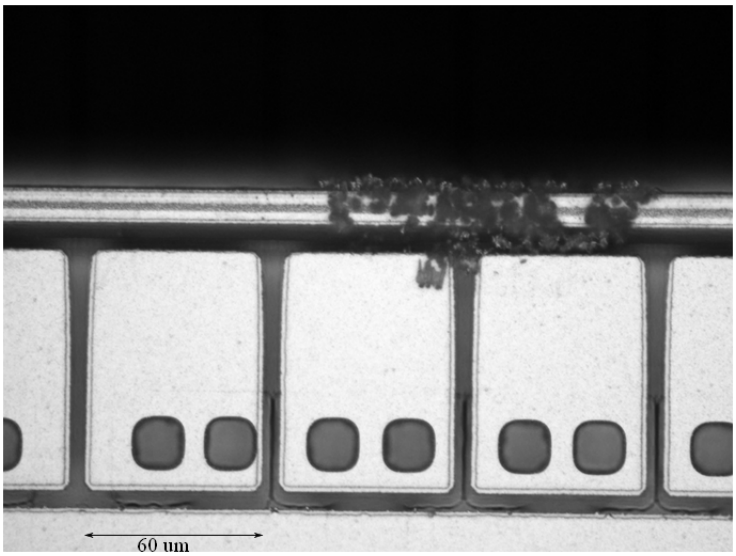

Figure 68: Micrograph of thin layer on the tested trap. It is from the residue of Si, oxide, Al, and photo-resist on the RF rail and DC electrode. This most likely, is the cause of the trap not working.

5. When the trap was taken out of UHV system and electrically validated, it was noticed

that the resistance between the DC electrodes and bond pads were higher than other traps with comparable dimensions. The resistance measurement ranged between 50 Ω and 400 Ω as compared to the resistances less than 5 Ω in typical cases for previous surface traps. Initially, the high resistance was linked to be the source of a disruptive RF phase difference caused by RF pick-up on the DC electrodes. This type of pick-up can cause effective fields at the ion location that cause severe micromotion and ion instability. Additionally, the phase difference can cause a moving RF null, making it impossible to trap ions [91, 92]. Later, after careful calculations, it was determined that the field generated by the unexpectedly high via resistance at the ion location would cause the Doppler modulation index β increase to $\beta \sim 0.5$ in the worst case. This is only a factor of three more than the traps having order of magnitude less resistances at the DC electrodes. Experimentally, $\beta \sim 0.5$ is not difficult to compensate and should not have prevented ion trapping. However, it may have contributed to the unsuccessful search for trapped ions.

8.3 The surface-electrode trap Gen III testing results

Since the UHV system built for the experiment was being used for the first time with an untested trap, it seemed reasonable that the optimized operation of the entire testing system should be demonstrated using a previously tested surface trap with well known characteristics. A "Gen III" surface-electrode trap previously tested in a well-characterized testing system was installed in the new symmetric trap testing system [89]. The cross-section and an SEM image of the Gen III trap are shown in Figure 69(a-b). Originally the Gen III trap was packaged on a carrier, which did not have laser machined holes on the corners where the top shield was to be installed. A new top-shield was designed for the Gen III trap testing. The top-shield used for this trap is shown in Figure 53(b) in Chapter 7. Once the trap with this shield was installed in the system, it was baked at 200°C for 8 hours and at 180°C for 64 hours. Since the primary reason for the Gen III testing was to verify

the system and laser angles, the leak-valve and ultra-low pressure ion gauge was removed from the UHV system. The pressure in the chamber could still be measured by the ion pump controller. Typically, when a UHV chamber is vented, the Ca oven is replaced. The Ca becomes oxidized in a couple of hours and typically the trap swapping operation takes long enough to require a replacement of oven. For this trap a new Ca oven was made and installed. The oven design was same as the one used in the first phase of the experiment and it is shown in Figure 54(a) in Chapter 7.

The electrical verification of the trap went as expected and matched the verification that was carried out a few months ago on a different system for this trap. For this testing, the system was re-arranged and the lasers were moved to be guided into the system from the front of the trap (as shown in the layout Figure 65). First, the neutral fluorescence was observed at an oven current of 2.7 A and persisted until the oven current was decreased to 2.1 A. For the beam orientations in this system, Doppler shifts reduce the optimum fluorescence wavelength from 423 nm to 422.79211 nm. The ion was trapped with the DC voltages applied as modeled. The layout of the trap and the location, where the ion was trapped, is shown in Figure 69(c). An image captured by a CCD camera of a four-ion uniform linear chain is shown in Figure 70. The initially trapped ion had micromotion that was nulled by applying approximately -1300 V/m in y-direction. That means a positive stray field of 1300 V/m was present that had to be compensated. The ion was coalesced at a laser detuning of 20 MHz below the cooling transition resonant wavelength of 397 nm.

The trapping RF voltage was calibrated by determining the voltage step-up of the resonator circuit as described in the RF resonator section. However, the actual applied RF voltage can only be obtained by measuring the ion radial mode frequencies and using the equation [65]

$$\omega_r = \frac{eV_0}{\sqrt{2}\Omega_{RF} m R^2}, \tag{95}$$

where R is the effective distance scale dependent on the geometry of the trap, Ω_{RF} is RF frequency, V_0 is the peak RF voltage, e is charge of an electron, and ω_r is the radial mode

frequency. For the Gen III trap R = 178 μm . The degenerate radial mode frequency was measured to be 3.2 MHz. For $^{40}Ca^{+}$ and RF cavity-resonance frequency of 65.05 MHz, V_0 is 55 V. To trap a linear four-ion chain shown in Figure 70 the potentials applied on various DC electrodes are given in the Table 14. The electrode identification numbers are shown in Figure 69(c).

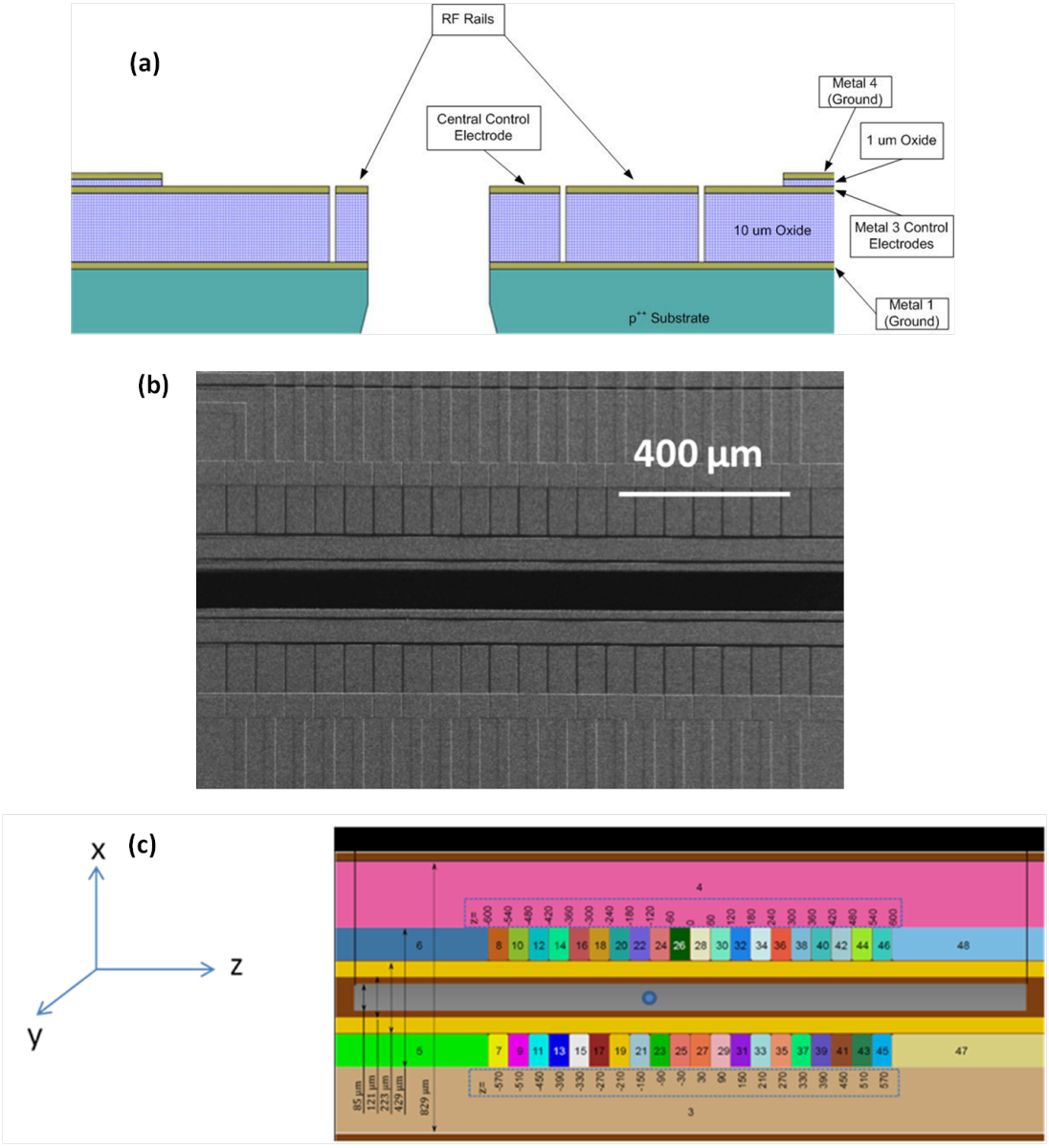

Figure 69: Gen III surface-electrode trap and relative trapped ion position.

The radial mode frequency of single-ion can be measured by a technique called ”DC

tickle" [65]. Typically DC tickle is done by applying a RF signal to one of the DC electrodes near the ion. Since this trap has a top shield that can generate an applied field over the entire trap surface; the RF source was applied to the shield at low amplitude (-20 dbm to -10 dbm). The frequency was swept to measure the mode frequency. At the radial mode frequency, the ion motion resonates with the applied RF fields. This excitation heats the ion and as a result, a decrease in fluorescence is observed. The measured radial-mode frequency of 3.2 MHz matches the static numerical simulation model.

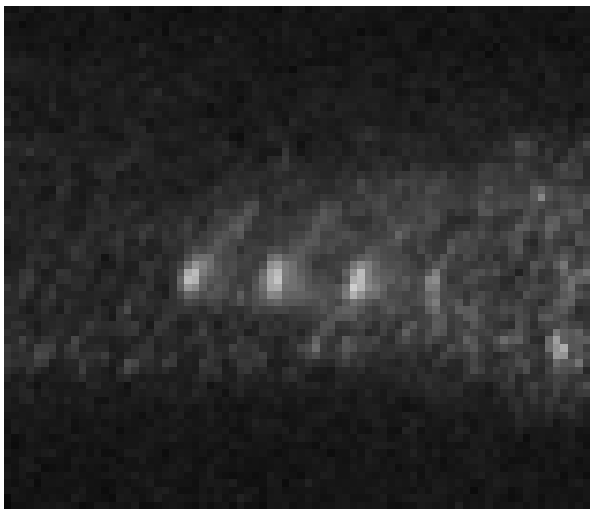

Figure 70: Uniform linear four-ion chain of $^{40}Ca^{+}$ trapped in a surface-electrode Gen III trap. The chain of ions was trapped at the RF frequency of 65.05 MHz, RF peak voltage of 45 V. The corresponding trapping DC potentials are given in Table 14.

Table 14: DC potentials for trapping a $^{40}Ca^{+}$ four-ion chain in Gen III trap. For a complete waveforms see [89].

DC electrode no.	23	24	25	26	27	28	29	30
Voltage (V)	3.42	3.39	-2.6	-2.6	-3.7	-3.7	3.2	3.19

8.4 The generation B symmetric trap testing results

The generation **B** symmetric traps were completed in April 2012. The first trap chip identified as "Symm 1 F6" was tested successfully during May-July 2012. The improvements made in the layout of generation **B** traps (discussed in Chapter 6 Section (6.4)) required

several modifications in the setup. These modifications are listed below:

- Because of the added bond pads the wire-bonding layout was modified accordingly. The wire-bonding layout shown in Figure 65 include these changes.

- The resonator cavity was modified to operate at 40 MHz instead of 60 MHz in previous two phases of the experiment. The modified resonator is shown in Figure 60 is the modified resonator. The resonator was modified to operate the trap on lower RF frequency.

- A new oven-shield was designed and installed. This new oven-shield design in shown in Figure 55(b) in Chapter 7. Due to the new oven-shield geometry the oven had to be installed farther away from the back-side of the trap.

After the trap was packaged using the procedure described in Section 8.1, the capacitance of the trap DC electrodes were measured. The capacitances were verified before and after the chamber bake-out. The capacitance measurements are listed in Appendix Table 18. In first column the carrier pad number corresponding to each electrode number is given and in the third column the electrode identification number for each DC electrode is given (see Figure 71). In Appendix Table 18 the electrode number 13 is highlighted in gray to indicate that this electrode is shorted to ground. This defect is caused by a mistake in the mask layout of M4 layer. The bond-pad corresponding to the DC electrode 13 remains connected to the top ground (M4) in the mask layout.

After the successful electrical verification of the trap and baking the system out to achieve a pressure in low 10^{-11} Torr range, the UHV system was placed on the optics table and the cooling and photoionization lasers were aligned through the top slot.

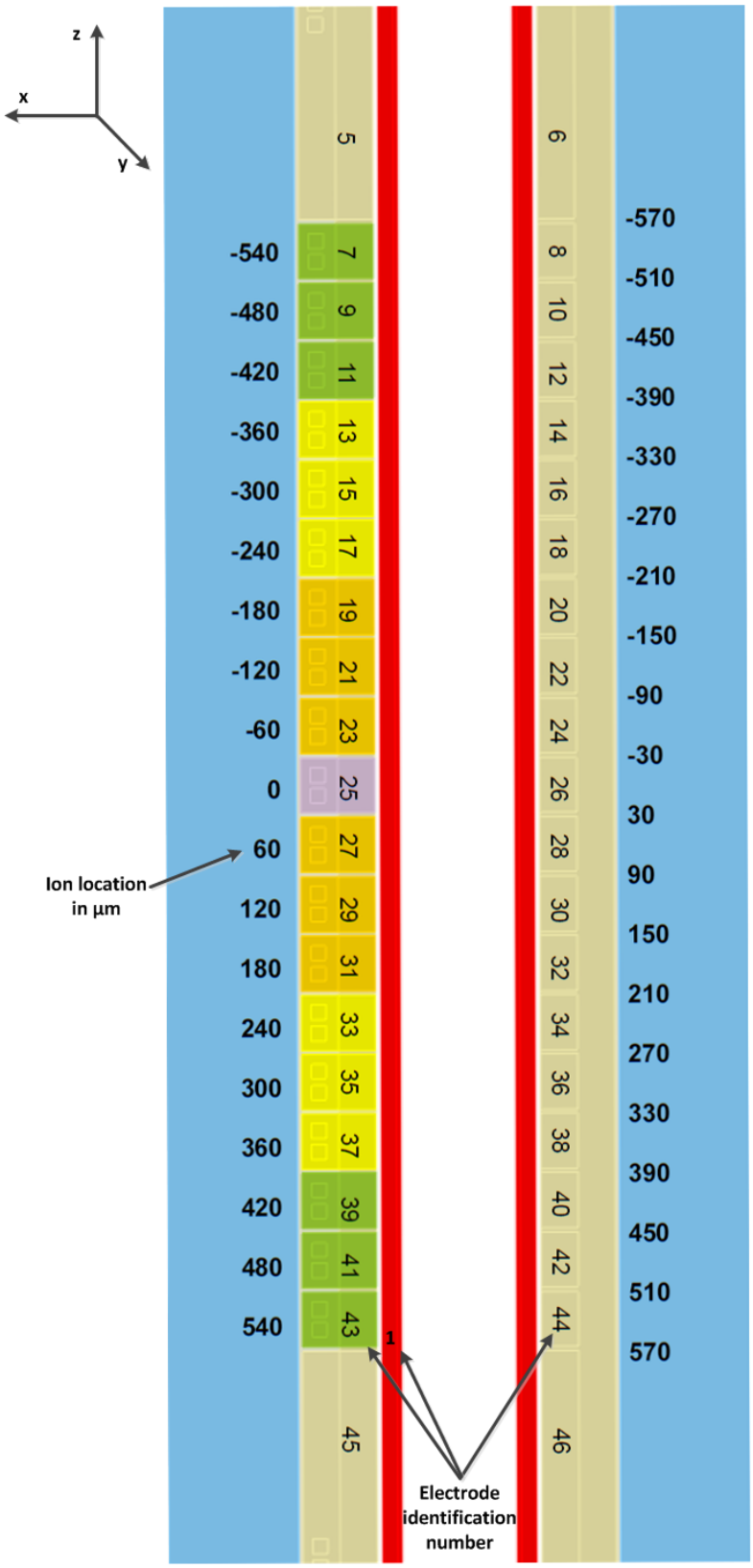

Figure 71: Electrode identification numbers used for the potentials application for the symmetric trap. The reference axis system and the reference ion positions are identified on the symmetric trap layout.

8.4.1 Trap testing results

The DC-electrode potentials for the symmetric trap were calculated using the BEM simulations of a realistic model. The realistic model of the trap was created by making two modifications in the ideal model. The DC-electrode 13 was shorted to ground and the back-side dimensions of the trap were modified according to the measured dimensions. The back-side of the fabricated trap (shown in Figure 72) has more SiO_2 material exposed than the designed trap. This was a result of the unexpected process variation that occurred during the back-side Si-etch process. The Si profile near the back-side ground metal has rough profile as shown in Figure 72. It will be clear from the results presented in the following discussion that this over-exposed dielectric material charges-up causing undesired stray fields that are hard to compensate. From the modified BEM model accounting for these two major deviations from the design, the DC potentials were calculated to trap ions across the entire trapping region. In the Table 15 a sample set of potentials are shown that are applied on a set of DC electrodes to trap an ion at the location $z = -90$ μm . The direction of the z-axis is shown in the Figure 71.

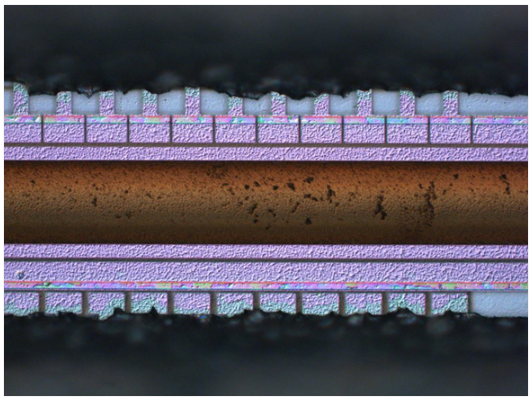

Figure 72: Micrograph of the back-side view of the sample taken from the generation B trap wafer. The image shows the exposed oxide due to over-etch Si and loss of M1 from the back-side of the trap.

During the testing of this trap we were able to load $^{40}Ca^{+}$ ion at multiple locations and shuttle ion for approximately 15 μm in each direction of the z (see Figure 71). This shuttling was limited by the cooling beam waist. The trapped ion images captured by a

CCD camera are shown in Figure 73. In the Figure 73(a) the ion image is overlaid on a trap laser-illuminated image maintaining the respective scales. In the Figure 73(b) another ion image is shown.

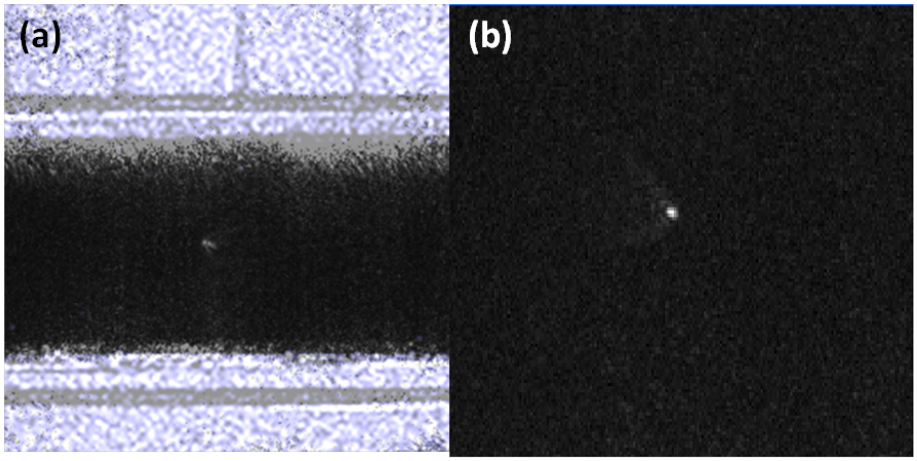

Figure 73: Images of a single-ion trapped in the symmetric trap. In (a) an CCD image of a trapped ion is overlaid on a laser-illuminated image of the trap maintaining the relative scales. In (b) a CCD image of a trapped ion with reduced background noise is shown.

8.4.1.1 Ion loading DC potentials

The DC potentials are calculated for trapping an ion at any location between z =-480 μm and z =480 μm . These base waveforms are calculated to produce an axial harmonic well with axial ion frequency ω_z = 1 MHz. While applying these waveforms at a particular location, the strength of the harmonic potentials can be scaled by multiplying a factor to the potentials applied. These base waveforms also provide the necessary axis rotation. The axis rotation allows cooling the ions with laser beams at a given angle to the trap surface. A vertical field was empirically found to be necessary to load. To load single ions in this trap a combination of the base waveforms and vertical field was used. The vertical field waveforms are set of uniform x and y fields which can be scaled independently to load at a particular location. To compensate the micromotion with a loaded ion these x and y waveforms are scaled accordingly. In the Table 15 the base waveforms and the x, y, and z waveforms for the location z = 90 μm are given. The x, y, and z waveform is scaled according to the measured stray fields for various location. These measured stray fields are

shown in Figure 74 and Figure 76. From the numerical simulations, the scale factor of 1 is determined to be producing 1000 V/m field in x or y or z directions. The scale factors are simply applied to the corresponding vertical field waveforms. These waveforms are

Table 15: DC potentials for trapping a $^{40}Ca^{+}$ ion in the symmetric trap at location z=-90 μm . To trap an ion at a particular location the potentials are applied with the scale factors multiplied with the vertical waveforms in each direction. As an example, to trap an ion at z=-90 μm the potentials are applied using the formula: Base waveform*2 + E_x waveform*(stray field compensation from Figure 74 based on ion position)/1000 + E_y waveform*-2.05 + E_z waveform*(stray field compensation from Figure 75 based on ion position)/1000.

DC electrode no.	17	18	19	20	21	22	23	24	25	26	27	28
Base waveform (V)	0.33	1.28	0.70	1.75	-1.23	-1.88	-1.28	-1.94	0.72	1.78	0.35	1.31
E_x waveform (V)	0.47	-0.52	0.47	-0.52	0.47	-0.52	0.47	-0.52	0.47	-0.52	0.47	-0.52
E_y waveform (V)	-0.26	0.38	-0.26	0.38	-0.26	0.38	-0.26	0.38	-0.26	0.38	-0.26	0.38
E_z waveform (V)	1.88	0.24	1.79	0.68	0.36	1.92	-0.27	-1.87	-2.2	-0.98	-1.32	0.26

calculated for $^{40}Ca^{+}$ ion loading with the realistic model, an RF frequency of 44 MHz and an RF peak voltage of 60 V.

8.4.1.2 Micromotion compensation

The extrinsic or excess micromotion in ion traps is caused by the external stray fields as discussed in Section 3.5. One of the common sources of these stray fields is charged dielectric material near the trapped ion when lasers are applied on the ion site. The fringe laser field can charge the dielectrics. Due to the proximity of these charges the ion micromotion is increased. One of the several advantages of the symmetric trap design is that there is no line-of-sight oxide exposed the ion. However, during the generation **B** trap fabrication process, the back-side clearance of the slot resulted in some exposed oxide (See Figure 72). Because of this exposed oxide, which can charge up while aligning the lasers, the trapped ion in this trap experience excess micromotion with amplitude up to a micron. For $^{40}Ca^{+}$ ion trapped at 44 MHz RF frequency with 60 V peak voltage, and a radial frequency of 6.3 MHz a stray static field of 3000 V/m can cause the micromotion with the

amplitude of 933 nm (using equations (19)). During our trapping experiment on this symmetric trap we were able to measure micromotion by compensating it. The micromotion was compensated by applying the electrode potentials that create field that opposes the stray field present at the ion site. The stray fields were measured in x, y and z directions (See Figure 71 for the directions.) The compensating fields applied to the trap electrodes in x and z directions are given in Figure 74 and Figure 75. The fields are measured at the trapping sites between $z = -90\ \mu$m and $z = 410\ \mu$m in 10 μm steps.

To compensate the micromotion in the x direction, the peak RF voltage is varied while keeping the axial trapping and other parameters constant. When the peak RF potential is varied the ion moves in x direction if the ion is not micromotion compensated in x direction. This motion can easily be detected by a PMT or a camera. Depending upon the direction of the stray field the ion can move in the corresponding direction along the x-axis. We were able measure the E_x stray fields up to 4000 V/m (Figure 74) with the resolution of the 300 V/m stray field.

To compensate the micromotion in z direction, the axial trapping strength is varied to see if it effects the ion null position in z-axis. Given the base waveforms that contain the potentials applied on a set of DC electrodes to create an axial harmonic null along the z-axis at a particular location, the null can be shifted in the presence of stray fields in axial direction. To compensate z micromotion, a uniform z potential is applied so that the ion does not move as axial harmonic potential is scaled.

To measure the stray fields in the y direction the micromotion induced sidebands on the resonance fluorescence spectral profile are mapped. When the ion sees a near zero stray field the fluorescence spectruum falls uniformly to zero as the cooling laser is tuned to the low frequency side of the resonance as shown by the orange curve in Figure 76 for a compensating field of -2800V/m. As micromotion increases with increasing uncompensated y field, a fluorescent sideband develops as shown by the peak near 44 MHz detuning for the red and blue curves in Figure 76.

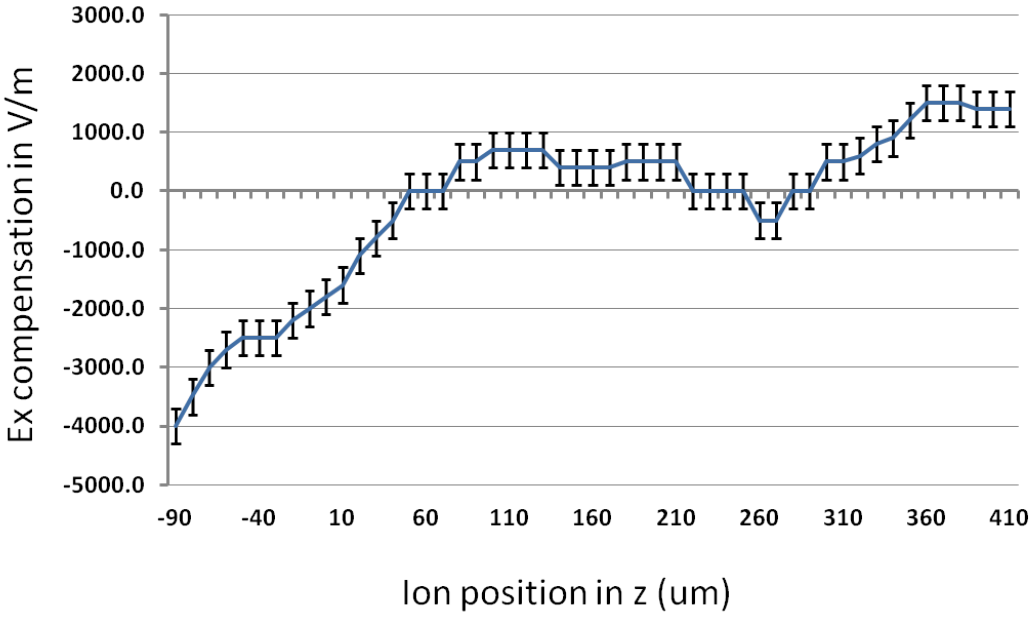

Figure 74: Stray fields in x-direction measured in V/m along the trapping region.

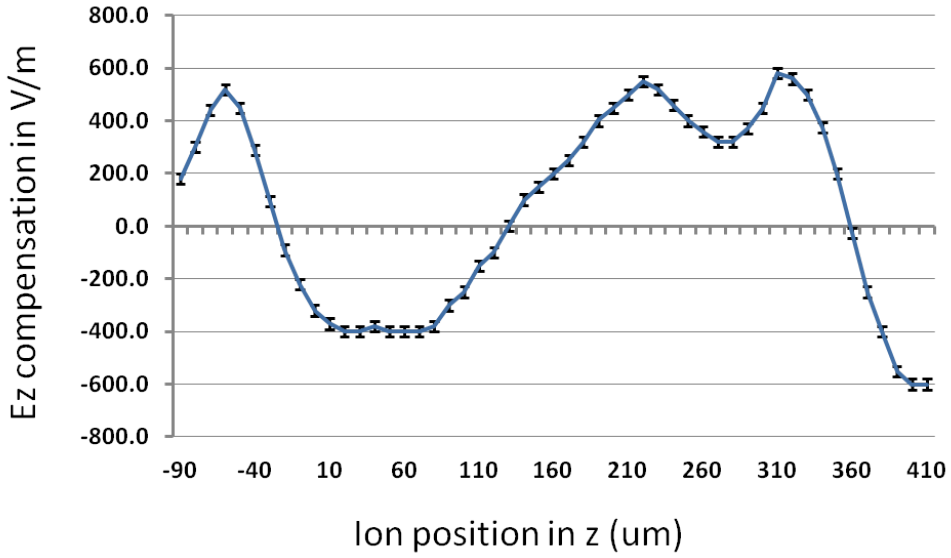

Figure 75: Stray fields in z-direction measured in V/m along the trapping region.

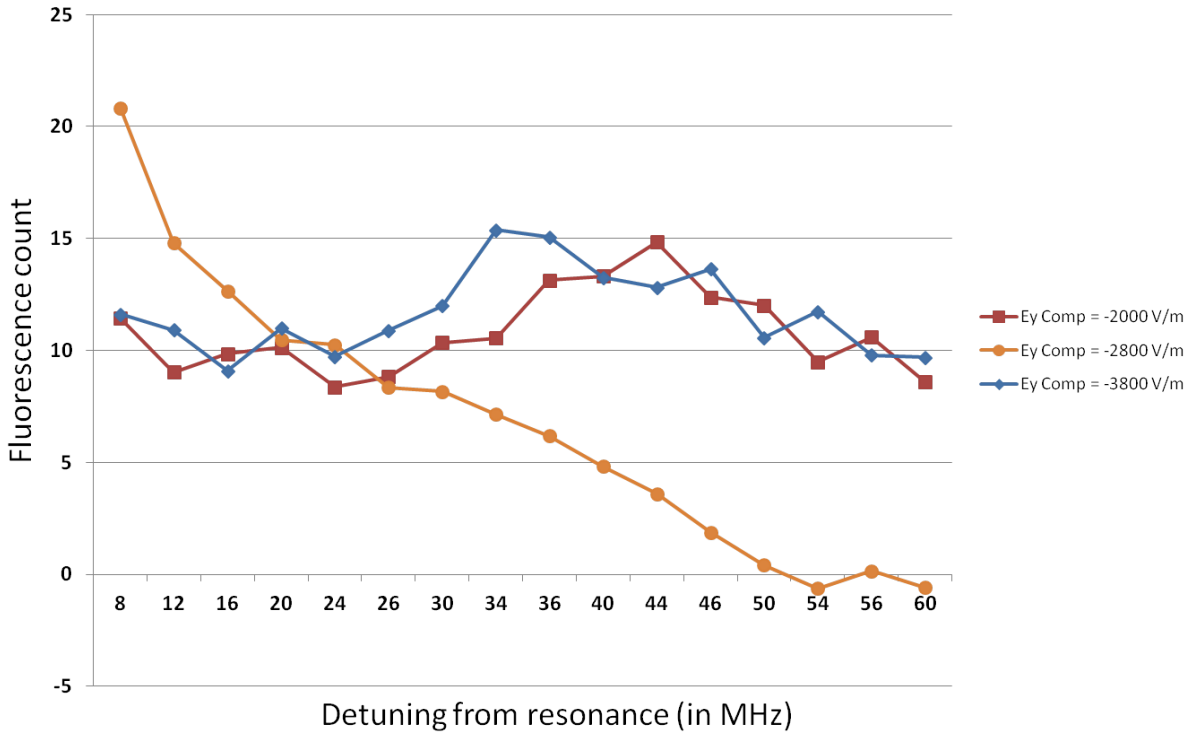

Figure 76: Ion fluorescence count varying with different E_y compensation fields. The compensation fields are in V/m. The micromotion sidebands are obvious when the ion is not compensated optimally. First micromotion sideband is obvious with the fields E_y =-2000 V/m and E_y =-3800 V/m at the RF frequency 44 MHz.

8.4.1.3 Mode measurement

When ions are trapped in the pseudopotential well created by RF and DC quadrupole, the ions have radial vibration frequencies. Near the center of the trapping region the pseudpotential is cylindrically symmetric and the radial mode frequencies along the x and y directions are typically equal. In some quantum simulation experiments, the splitting of the x and y the radial mode frequencies is desired. This splitting can be achieved by applying a DC bias on the RF electrode or offsetting the voltages on DC electrodes. Typically, trap operating conditions are chosen to keep $q < 0.4$. The radial-mode frequency for the symmetric case is given by $\omega_r = \frac{q\Omega_{RF}}{2\sqrt{2}}$, where Ω_{RF} is the RF frequency. The mode frequencies (radial and axial) can be measured by applying small resonance excitations to the ion using RF voltages applied to nearby DC or RF electrodes. In this experiment, the shield above the trap is used to excite the radial trap modes. Excitation of a mode is observed as a decrease

in the ion florescence while it is being laser-cooled. The change in the fluorescence can be observed by CCD camera capturing the integrated light. When the measurements are done a statistically significant number of times, the mode frequencies can be measured quite accurately to within a few tenths of a megahertz. The stability of these mode frequencies is a good indicator of the stability of the trap fields and variations that occur due to electrode charging from such sources as the laser beam fringes striking the electrode surfaces.

The radial modes measured at various locations in the symmetric trap are given in Figure 77. The radial secular frequencies are measured using this technique called "DC-tickle". Using the equation (95) and the measured radial modes, the calculated RF peak voltage is 56.6 V. Where the trap geometry parameter R calculated from the BEM model is $R = 94\ \mu$m . With the radial modes of ω_1=9.9 MHz and ω_2=6.3 MHz, the calculated q=0.4. The radial frequency of 6.3 MHz and $q = 0.4$ confirm our simulation results. However, the measured radial mode 9.9 MHz and the splitting can be explained by the curvature in the stray fields that forces the parameters a_x and a_y to be high and different from each other. From the calculations the values for stability parameters a_x and a_y are at two different values of 0.2 and 0.37. These higher values include the DC components added by the bias created on the RF electrode due to stray fields. Although these trapping parameters are not optimal they show that the the trapping is strong enough to sustain the high stray fields owing to the trap's symmetry and deep trapping characteristics. For QS experiments this splitting is useful. Because of the splitting it is easier to couple only one of the radial modes with sufficient control.

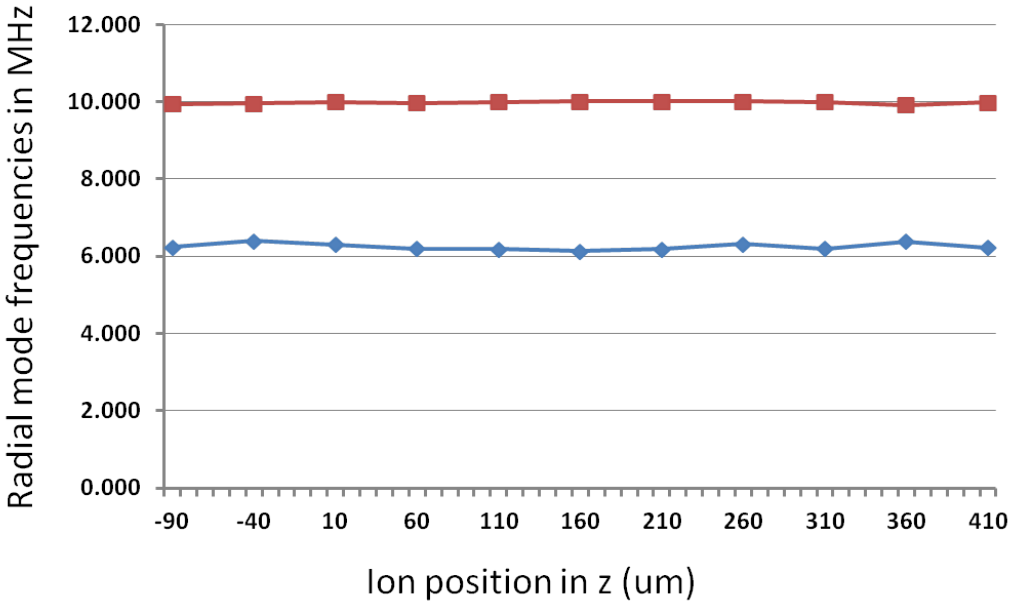

Figure 77: Measured radial modes of an ion trapped at different locations in the symmetric trap. The radial frequencies are measured to be 10 MHz and 6.3 MHz.

8.4.1.4 Lifetime measurement

A trapped ion in this trap remained trapped for several hours if it was cooled continuously. However, for a typical quantum simulation experiment the trapped ion has to remain stably trapped for more than one second without being cooled. The dark lifetimes of the trapped ion in this trap were measured by shutting off the cooling beams for one to ten seconds. From the measurements it can be concluded that the trapped ion survives 100% for one to four seconds and with lower probability it survives up to ten seconds.

Table 16: Dark lifetimes of the ion trapped in the symmetric trap measured with ten samples of loaded ions for each row of data. The survival chance is a rough indicator of the lifetimes of the ion for each time interval.

Time (in secs)	Survival chance (%)
1	100
2	100
3	100
4	100
5	80
6	50
7	30
8	20
9	20
10	10

8.5 Improved experimental setup for generation B trap testing

During the testing of "Symm1 F6" in third experimental phase, a slow loading rate of the ions was observed. Typically, when ion is loaded, the photionization beams are blocked and the atomic oven is turned off. Blocking the atomic flux avoids any collisional loss of the trapped ion. If the loading rate is equal or higher than the collisional loss rate, multiple-ion loading becomes challenging. In the third experimental phase, the atomic oven was installed so that the atomic beam was perpendicular to the trap surface. Therefore, the angle between the photoionization beam and the atomic beam was 135°. Because of that the linewidth of the photonionzation transition was Doppler-broadened to 1 GHz and the probability of the photoionization was decreased. The loading rate of 1-ion per 20 s was observed. This loading rate was measured to be equal to the ion loss rate due to the atomic oven flux. This implied that the ion/atoms ratio was too low to allow multiple ion loading. To have an optimal photoionization rate, the photoionization beam and the atomic beams should be perpendicular to each other. By having orthogonal ionizing beam and Ca beam, a minimum number of atoms have the velocity compnents along the axis of the ionization beam resulting in minimum Doppler broadening. This reason was the primary motivation

to redesign the UHV chamber and laser setup in such a way that there is 90° between atomic beam and 423 nm ionization beam. This increases the ionization rate (ions/atom ratio) by a factor of four.

In the new UHV chamber following modifications were made:

- New oven and oven shields were designed to accommodate angled installation of the oven on the back-side of the trap. On the back-side of the trap, the 100 socket wires are routed to create a room for the oven-shield and oven installation. The new oven assembly includes an extension tube that is installed to guide the oven flux. The oven flux guiding tube, new oven-shield, and the new angles are shown in the Figure 78(a).

- The socket is rotated 90° to make room for the oven-shield and oven installation. The cross-section shown in Figure 78(a) shows the rotated socket orientation. In the new system, the trap slot's longer side is perpendicular to the optic table surface.

- A new trap spacer is designed to accommodate angled atomic flux. In the spacer design used in previous experiment (shown in Figure 62), the oven flux entering at an angle from the back-side can short the RF-DC electrodes by allowing the atomic flux to form a thin metallic layer of Ca. The new spacer design and angled atomic flux guiding tube are shown in Figure 78(b).

These modifications inside the the UHV chamber along with a new setup of the 423 nm and 377 nm laser beams path provide the angle between the atomic beam and the laser beams of 85°(shown in Figure 78(a)). With this improved setup of the UHV chamber and the lasers, the Doppler broadening of the natural linewidth of the photoionization laser is closer to the minimum. The measured broadening of the 423 nm linewidth with this new setup is 100 MHz. With this new setup the neutral fluorescence has successfully been observed. The system is currently installed with a new trap from the wafer "Symm2" and the chip ID "F4". This trap does not have a defective shorted electrode that was present in

”Symm1 F6” trap chip in previous experiment. The efforts to trap an ion followed by the trapping of linear ion chain are ongoing areas of research in the QIS group of GTRI.

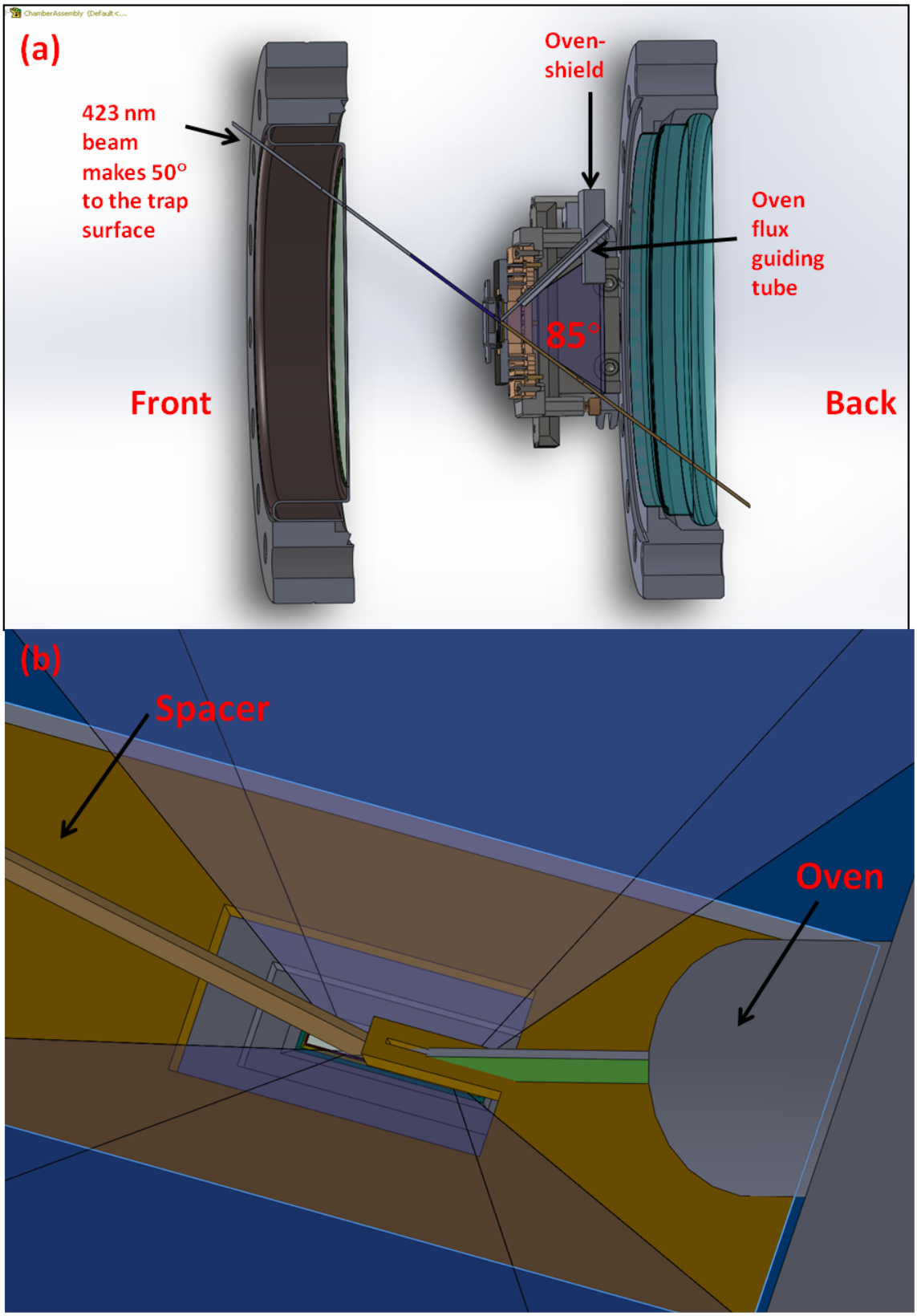

Figure 78: CAD drawings of the new experimental setup to test the symmetric trap. In (a) the cross-section of the configuration of the oven assembly and the lasers to form an angle of 85° is shown. In (b) a new spacer-shield designed for the angled atomic flux is shown.

CHAPTER 9

CONCLUSION

In this thesis, I demonstrated a hybrid design of a micro-scale ion trap that can be fabricated using Si-based CMOS technologies. For some quantum simulation experiments linear ion chains have to be stable and the ions' radial modes have to be split yet with stable frequencies. These conditions require the trap design to be micro-scale and yet provide symmetric radial confinement. Combining the characteristics of the micro-scale surface-electrode traps and miniaturized two-level traps, the new geometry structure

- offers deeper trapping potential,
- produces symmetric radial confinement,
- provides more optical access,
- avoids line-of-sight dielectric,
- contains the flexibility to apply DC potentials to compensate stray fields,
- possesses resilience to stray fields,
- can be be fabricated with repeatability and consistency using standard Si-based CMOS technologies.

This thesis work presented single-ion $^{40}Ca^{+}$ and $^{171}Yb^{+}$ simulation studies, fabrication processes and corresponding recipes, and the experimental demonstration of the working of the symmetric ion trap. This thesis lays the foundation for ongoing research of designing and testing a new kind of micro-scale hybrid ion trap that are inspired by this design. The symmetric trap discussed in this thesis is being used by the experimental groups for ongoing quantum simulation experiments.

CHAPTER 10

APPENDIX

10.1 The measured capacitance of the symmetric traps

Table 17: Capacitance (in pF) of the electrodes of selected symmetric trap chips. GND refers to the pads that are grounded using wire-bonds connecting them to carrier ground ring. The shaded gray cells represent the electrodes which were measured to be shorted to ground due to some defects. Pad 14 is RF electrode with capacitance only in 6-8 pF range. Rest of the electrodes have capacitances in the range of 55-65 pF.

Capacitance in pF				
Carrier Pad	**Socket Pin**	**Chip ID: F6**	**Chip ID: E7**	**Chip ID: E5**
1	B2	GND	GND	GND
2	B1	GND	GND	GND
3	C2	GND	GND	GND
4	C1	62	-1	62
5	D2	GND	GND	GND
6	D1	61	63	62
7	E2	62	62	63
8	E1	59	63	60
9	F3	GND	GND	GND
10	F2	61	63	62
11	F1	60	63	62
12	G2	GND	GND	GND
13	G3	GND	GND	GND
14	**G1**	7	6	6
15	H1	60	60	59
16	H2	63	59	60
17	H3	GND	GND	GND
18	J1	64	65	63
19	J2	63	120	63
20	K1	64	120	63
21	K2	GND	GND	GND
22	L1	65	61	61
23	M1	GND	GND	GND
24	L2	GND	GND	GND
25	N1	GND	GND	GND
26	M2	GND	GND	GND
27	N2	GND	GND	GND
28	M3	GND	GND	GND
29	N3	66	62	62
30	M4	GND	GND	GND
31	N4	67	-1	61
32	M5	68	61	59
33	N5	63	58	58
34	L6	GND	GND	GND
35	M6	64	57	58
36	N6	GND	GND	GND
37	M7	GND	GND	GND
38	L7	GND	GND	GND
39	N7	GND	GND	GND
40	N8	GND	GND	GND
41	M8	63	58	61

Continued on Next Page...

Table 17 – Continued

Carrier Pad	Socket Pin	Chip ID: F6	Chip ID: E7	Chip ID: E5
42	L8	GND	GND	GND
43	N9	62	57	60
44	M9	64	58	52
45	N10	62	-1	-1
46	M10	GND	GND	GND
47	N11	63	57	-1
48	N12	GND	GND	GND
49	M11	GND	GND	GND
50	N13	GND	GND	GND
51	M12	GND	GND	GND
52	M13	GND	GND	GND
53	L12	GND	GND	GND
54	L13	63	62	62
55	K12	GND	GND	GND
56	K13	62	60	60
57	J12	61	62	63
58	J13	60	63	-1
59	H11	GND	GND	GND
60	H12	61	60	60
61	H13	60	59	61
62	G12	GND	GND	GND
63	G11	GND	GND	GND
64	G13	GND	GND	GND
65	F13	61	58	61
66	F12	62	60	62
67	F11	GND	GND	GND
68	E13	62	59	61
69	E12	63	60	61
70	D13	63	59	62
71	D12	GND	GND	GND
72	C13	64	60	-1
73	B13	GND	GND	GND
74	C12	GND	GND	GND
75	A13	GND	GND	GND
76	B12	GND	GND	GND
77	A12	GND	GND	GND
78	B11	GND	GND	GND
79	A11	63	61	59
80	B10	GND	GND	GND
81	A10	62	60	61
82	B9	62	61	-1
83	A9	GND	GND	GND
84	C8	GND	GND	GND
85	B8	63	60	61
86	A8	-1	61	61
87	B7	GND	GND	GND
88	C7	GND	GND	GND
89	A7	GND	GND	GND
90	A6	GND	GND	GND
91	B6	63	61	60
92	C6	GND	GND	GND
93	A5	64	65	63
94	B5	65	62	65
95	A4	66	64	64
96	B4	GND	GND	GND
97	A3	62	63	61
98	A2	GND	GND	GND
99	B3	GND	GND	GND
100	A1	GND	GND	GND

Table 18: Capacitance (in pF) of the electrodes of selected symmetric trap chips. GND refers to the measurements that of the pads that are shorted to ground through connection to the carrier ground ring. The shaded gray cells represent the electrodes that were measured to be shorted to ground due to some defects. Pad 14 is RF electrode with capacitance only in 12-14 pF range. Rest of the electrodes have capacitances in the range of 50-82 pF.

Carrier Pad	Socket Pin	Electrode identification number	Capacitance in pF
1	B2		GND
2	B1		GND
3	C2		GND
4	C1	16	73.4
5	D2		GND
6	D1	14	71.7
7	E2	12	69.3
8	E1	10	74.7
9	F3		GND
10	F2	08	68.3
11	F1	06	66.3
12	G2		GND
13	G3		GND
14	**G1**		14
15	H1	05	69
16	H2	07	71.6
17	H3		GND
18	J1	09	76
19	J2	11	68.5
20	K1	13	-1
21	K2		GND
22	L1	15	78.3
23	M1		GND
24	L2		GND
25	N1		GND
26	M2		GND
27	N2		GND
28	M3		GND
29	N3	17	74.6
30	M4		GND
31	N4	19	75.3
32	M5	21	76.5
33	N5	23	75
34	L6		GND
35	M6	25	72
36	N6		GND
37	M7		GND
38	L7		GND
39	N7		GND
40	N8		GND
41	M8	27	74.8
42	L8		GND
43	N9	29	76.7
44	M9	31	71
45	N10	33	76
46	M10		GND
47	N11	35	82.5
48	N12		GND
49	M11		GND
50	N13		GND
51	M12		GND
52	M13		GND
53	L12		GND
54	L13	37	77.5

Continued on Next Page…

Table 18 – Continued

Carrier Pad	Socket Pin	Electrode identification number	Capacitance in pF
55	K12		GND
56	K13	39	74
57	J12	41	73.4
58	J13	43	68.2
59	H11		GND
60	H12	45	73.1
61	H13	03	69
62	G12		GND
63	G11		GND
64	G13		GND
65	F13	04	73
66	F12	46	66.7
67	F11		GND
68	E13	44	65.6
69	E12	42	71.5
70	D13	40	69.4
71	D12		GND
72	C13	38	69.8
73	B13		GND
74	C12		GND
75	A13		GND
76	B12		GND
77	A12		GND
78	B11		GND
79	A11	36	74.7
80	B10		GND
81	A10	34	71.7
82	B9	32	75.2
83	A9	30	GND
84	C8		GND
85	B8	28	72.7
86	A8		GND
87	B7		GND
88	C7		GND
89	A7		GND
90	A6		GND
91	B6	26	78
92	C6		GND
93	A5	24	79
94	B5	22	77
95	A4	20	81
96	B4		GND
97	A3	18	81
98	A2		GND
99	B3		GND
100	A1		GND

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